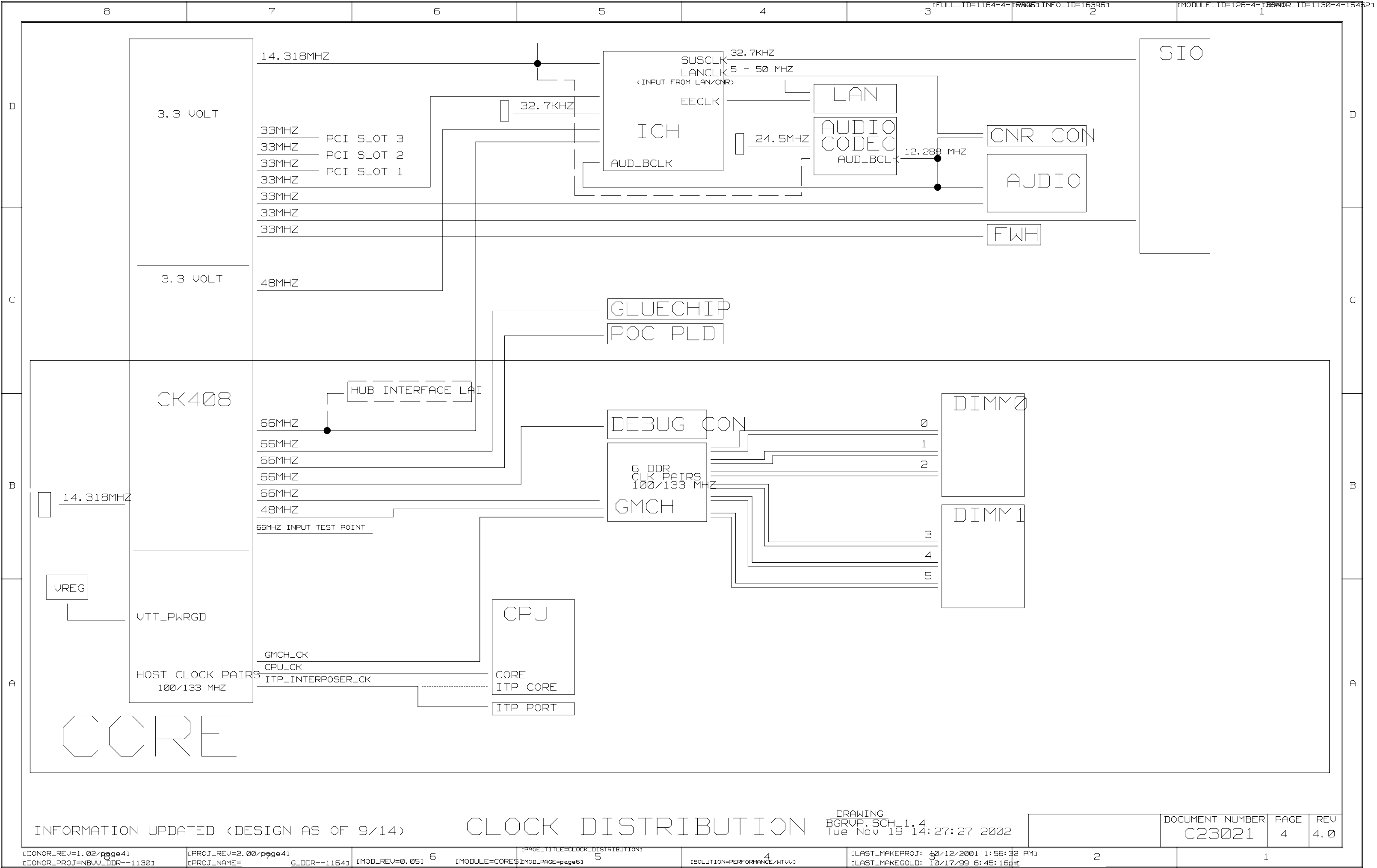


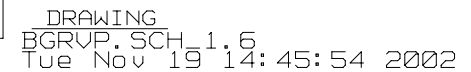
RESET MAP

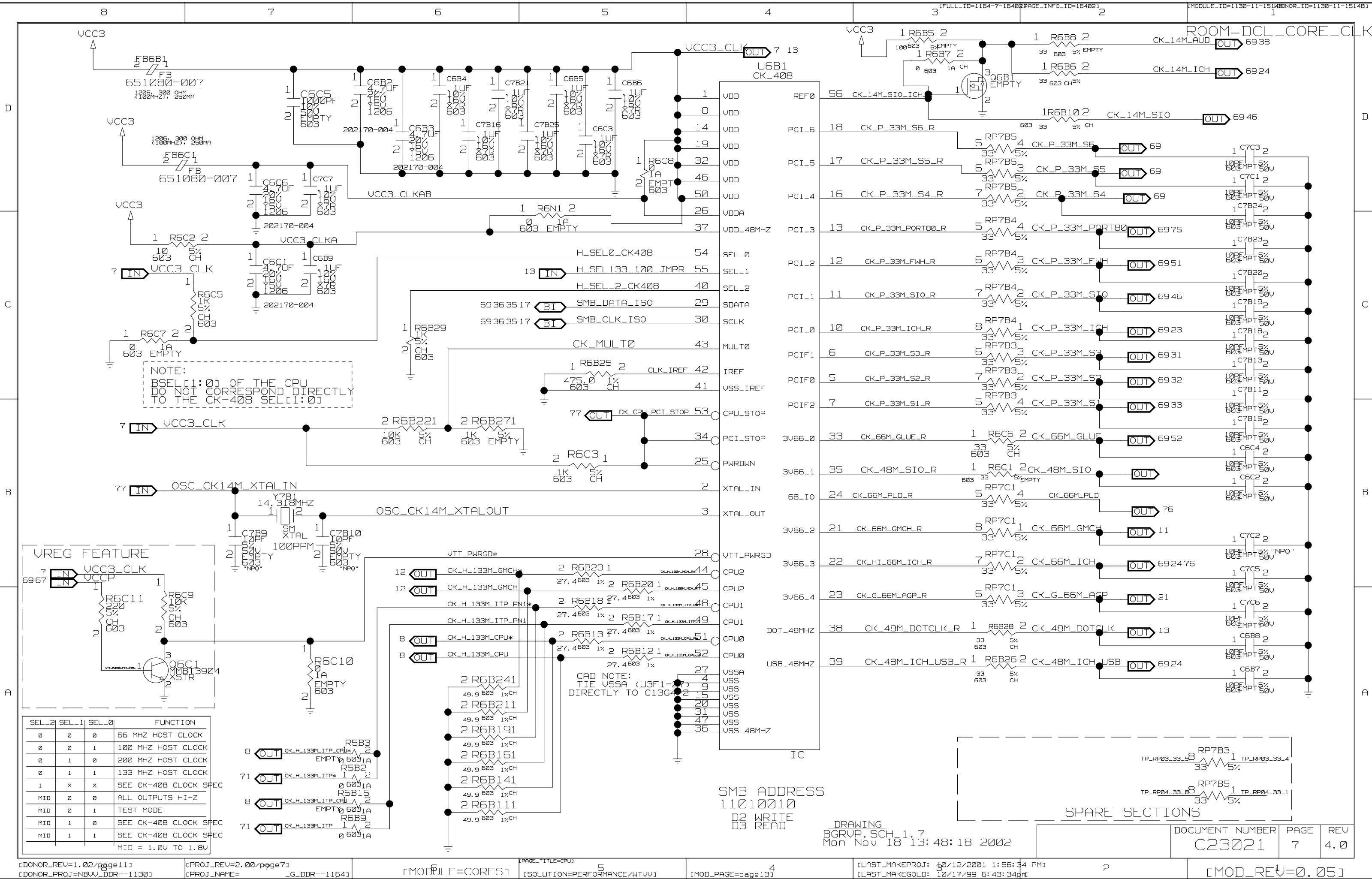
DRAWING
BGRVP, SCH 1.3
Mon Nov 18 13:06:37 2002

DOCUMENT NUMBER	PAGE	REV
C23021	3	4.0



8		7		6		5		4		3		2		1		[FULL_ID=1164-5-16398] [BGRUP_ID=16398] [MODULE_ID=128-5-16398] [BGRUP_ID=16398] [MODULE_ID=128-5-16398] [BGRUP_ID=16398]								
D	ICH4	ICH4					IRQ ROUTING TABLE									D								
		PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	INTERNAL PULL-UP	NOTES																
		GPI<0>	CORE	P_REQA#	---	---																		
		GPI<1>	CORE	P_REQ5#	---	---																		
		GPI<2>	CORE	P_IRQE#	---	---																		
		GPI<3>	CORE	P_IRQF#	---	---																		
		GPI<4>	CORE	P_IRQG#	---	---																		
		GPI<5>	CORE	P_IRQH#	---	---																		
		GPI<6>	CORE	UNUSED	---	---																		
		GPI<7>	CORE	UNUSED	---	---																		
		GPI<8>	RESUME	UNUSED	---	---																		
		GPI<11>	RESUME	SMB_ALERT#	---	---																		
		GPI<12>	RESUME	LPC_SIO_SMI#	---	---																		
		GPI<13>	RESUME	LPC_SIO_PME#	---	---																		
		GPO<16>	CORE	P_GNTA#	HIGH	OFF	24K																	
		GPO<17>	CORE	P_GNT5#	HIGH	OFF	24K																	
		GPO<18>	CORE	UNUSED	HIGH	OFF																		
		GPO<19>	CORE	UNUSED	HIGH	OFF																		
		GPO<20>	CORE	UNUSED	HIGH	OFF																		
		GPO<21>	CORE	ISA_GO_NOGO	HIGH	OFF																		
		GPO<22>	CORE	UNUSED	HIGH-Z	OFF																		
		GPO<23>	CORE	UNUSED	LOW	OFF																		
		GPIO<24>	RESUME	UNUSED	LOW	DEFINED																		
		GPIO<25>	RESUME	GPO_GRN_BLNK	HIGH	DEFINED																		
		GPIO<27>	RESUME	GPO_YEL_BLNK	HIGH	DEFINED																		
		GPIO<28>	RESUME	GPO_LAN_DISABLE	HIGH	DEFINED																		
C	ICH4	GPIO<32>	CORE	NO_POP*	HIGH	OFF																		
		GPIO<33>	CORE	UNUSED	HIGH	OFF																		
		GPIO<34>	CORE	UNUSED	HIGH	OFF																		
		GPIO<35>	CORE	UNUSED	HIGH	OFF																		
		GPIO<36>	CORE	UNUSED	HIGH	OFF																		
		GPIO<37>	CORE	<BOARD1>	HIGH	OFF																		
		GPIO<38>	CORE	<BOARD2>	HIGH	OFF																		
		GPIO<39>	CORE	<BOARD3>	HIGH	OFF																		
		GPIO<40>	CORE	<BOARD4>	HIGH	OFF																		
		GPIO<41>	CORE	UNUSED	HIGH	OFF																		
		GPIO<42>	CORE	UNUSED	HIGH	OFF																		
		GPIO<43>	CORE	CDC_DWN_ENAB*	HIGH	OFF																		
		RI*	RESUME																					
		THERM*	CORE																					
B	ICH4																							
A	F/W	GPI4		CONFIG JUMPER	INPUT	DEFINED		CONFIG JUMPER																
		GPI3		MANUF MODE	INPUT	DEFINED		MANUF MODE																
		GPI2		HI/LOW BIOS CONFIG	INPUT	DEFINED		SPARE HI/LOW BIOS CONFIG STRAP																
		GPI1		GPIO_DMA66_DETECT_SEC	INPUT	DEFINED		ATA66 CABLE DETECT - SECONDARY																
		GPI0		GPIO_DMA66_DETECT_PRI	INPUT	DEFINED		ATA66 CABLE DETECT - PRIMARY																
A	SIO																							
A	SIO	GPI020		RESISTOR STRAP OPTION	INPUT	DEFINED		DESIGN FEATURE WITH RESISTOR STRAPPING																
		GPI021		RESISTOR STRAP OPTION	INPUT	DEFINED		DESIGN FEATURE WITH RESISTOR STRAPPING																
		GP027/IOSMI*		IO_SMI*	INPUT	DEFINED		SENDS IO SMI REQUEST TO ICH2																
MULTI-PLEXED GPIO PINS ON SIO USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE UN-USED GPIO PINS ON SIO ARE NOT IDENTIFIED HERE																								
GPIO, IRQ, IDSEL MAPS																								
DRAWING BGRUP, SCH 1.5 Mon Nov 18 13:47:40 2002																								
DOCUMENT NUMBER C23021																								
PAGE 5																								
REV 4.0																								
[DONOR_REV=1.02/page5]		[PROJ_REV=2.00/page5]		[MOD_REV=0.05]		5		4		[LAST_MAKEPROJ: 10/12/2001 1:56:33 PM]		2		1										
[DONOR_PROJ=NBVV_DDR--1130]		[PROJ_NAME=--G_DDR--1164]		[MODULE=CORES]		[MOD_PAGE=page7]		[PAGE_TITLE=GPIO DISTRIBUTION]		[SOLUTION=PERFORMANCE/WTUV]		[LAST_MAKEGOLD: 10/17/99 6:45:18 PM]												





ROOM=DCL_CORE_CPU

D

C

B

A

D

C

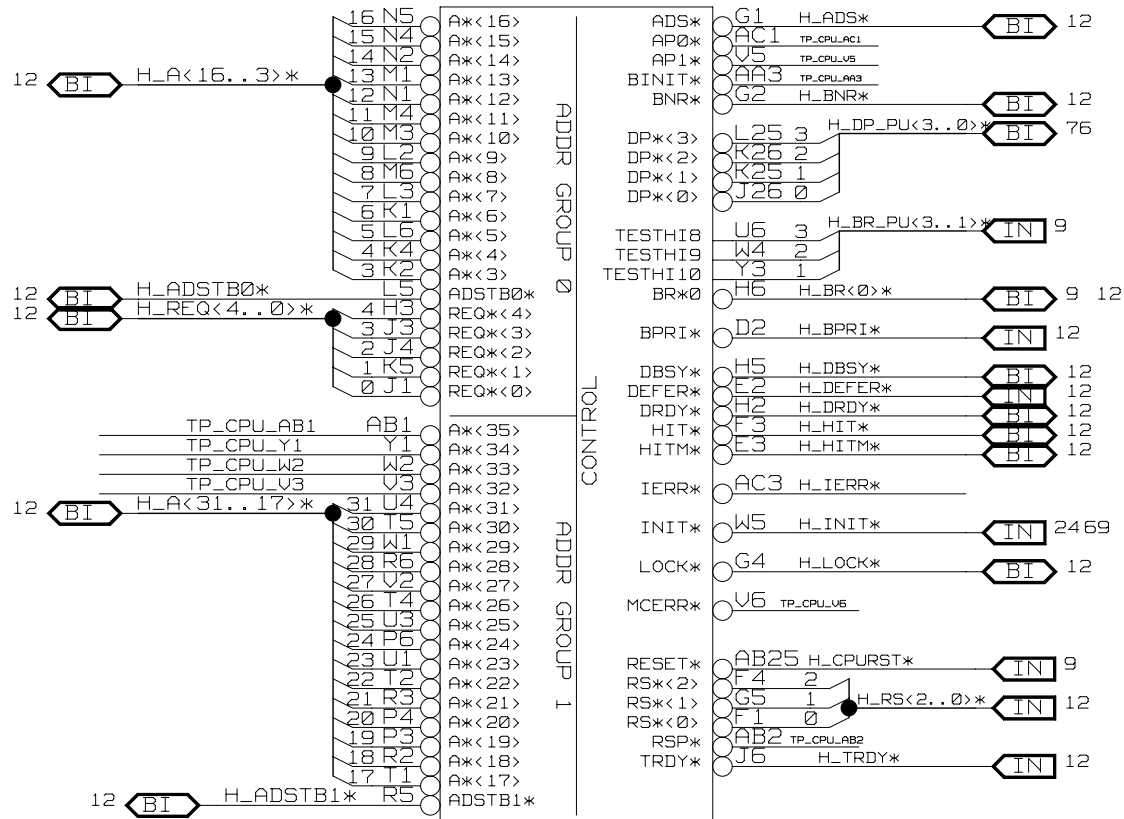
B

A

CPU

J2E1
NWD478

A16104-006



D

C

B

A

D

C

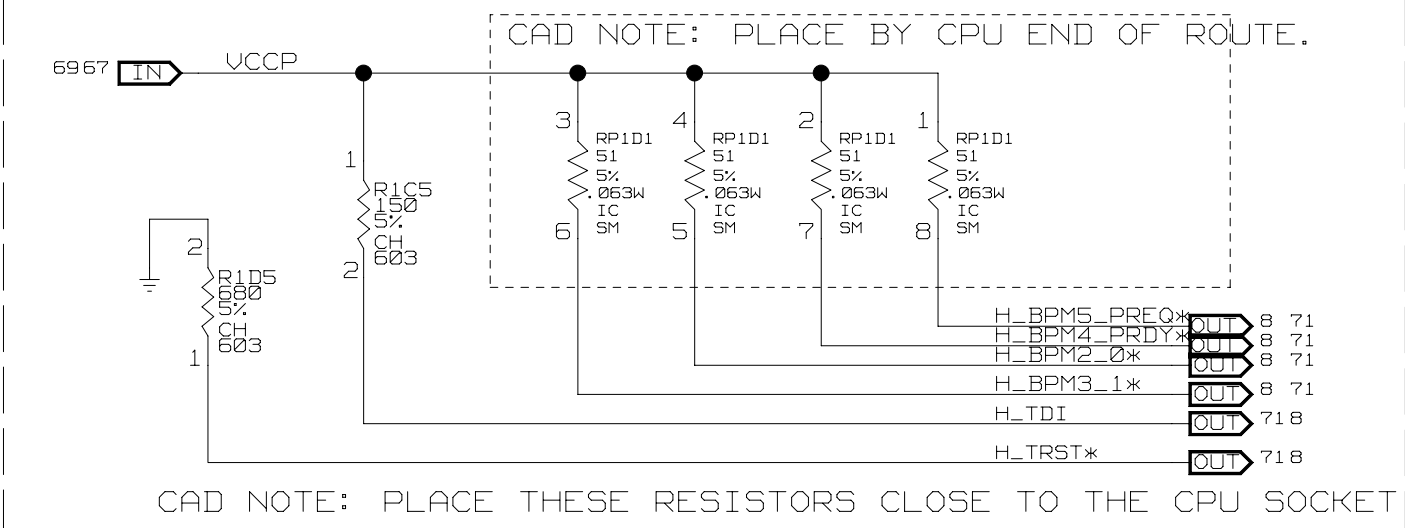
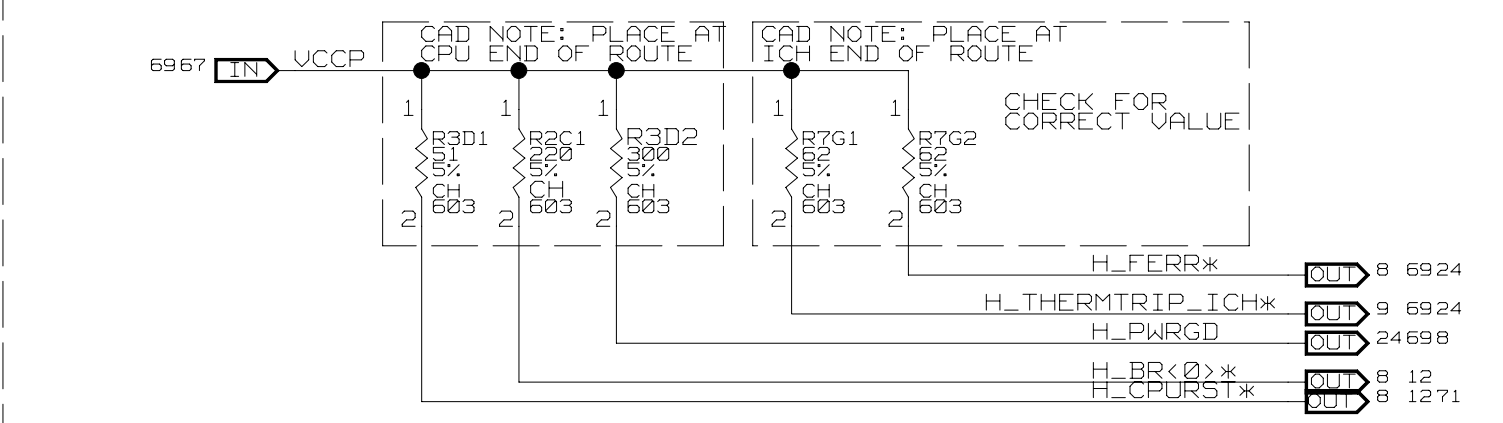
B

A

CPU SIGNAL TERMINATION

ROOM=DCL_CORE_CPU

ITP/TAP TERMINATION



TESTHI PULLUPS

TESTHI PIN NAME MAPPING

TESTHI[0] BYPASSEN

TESTHI[1] ODT

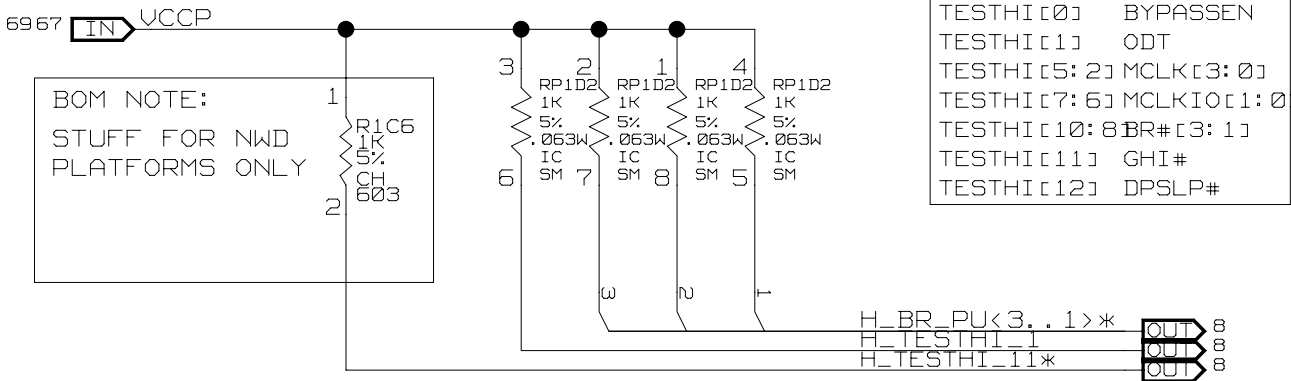
TESTHI[5:2] MCLK[3:0]

TESTHI[7:6] MCLKIO[1:0]

TESTHI[10:8] BR#[3:1]

TESTHI[11] GHI#

TESTHI[12] DPSLP#

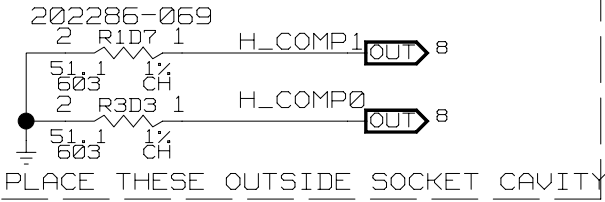


DESIGN NOTE: THESE CAN BE COST-REDUCED FOR PRODUCTION BY GROUPING [11], [10:8], AND [1:0] TO ONE PULLUP PER GROUP

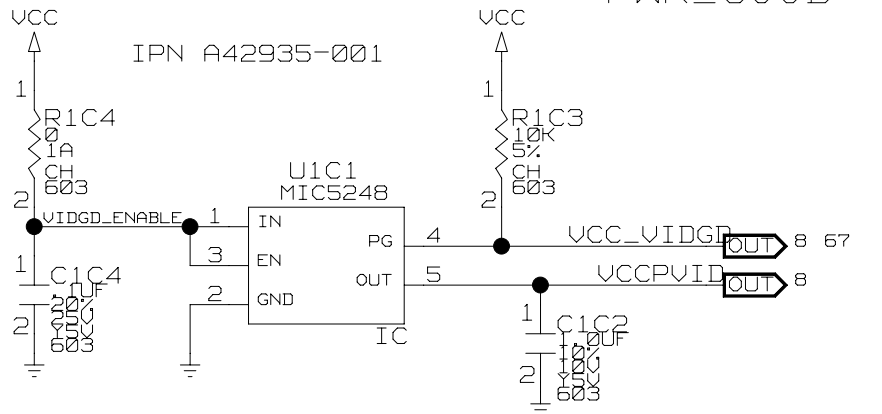


DEBUG ONLY

PRECISION FSB COMPENSATION RESISTORS

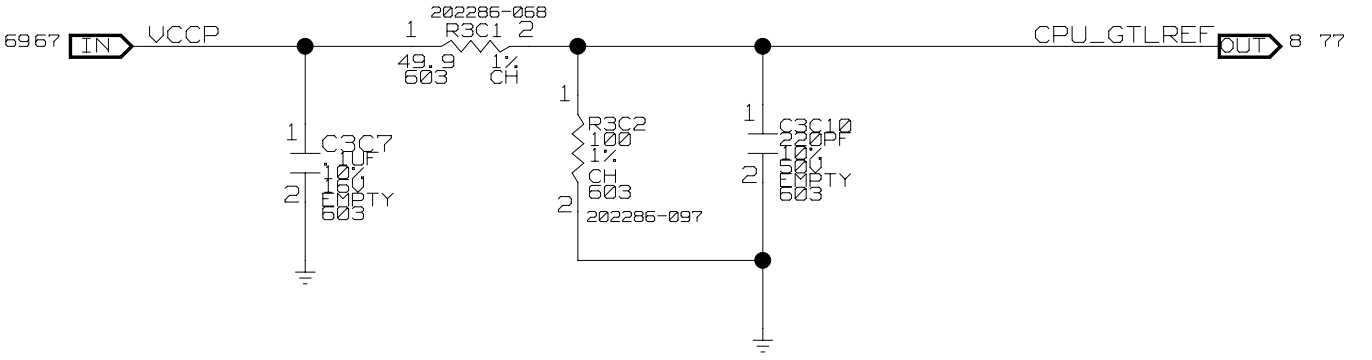


PWR_GOOD



PLACE NEAR PIN 5

GTLREF GENERATION CIRCUITS



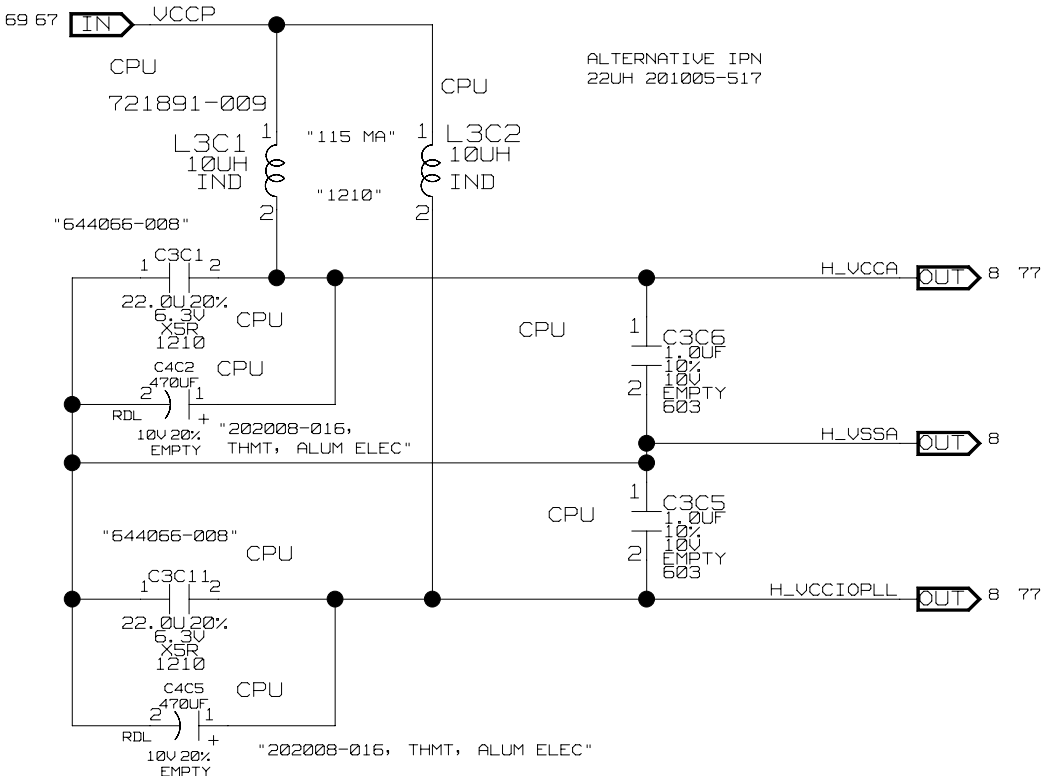
CPU PULLUPS/PULLDOWNS/TERMINATION

DRAWING
BGRUP.SCH_1.9
Mon Nov 18 13:48:08 2002

DOCUMENT NUMBER	PAGE	REV
C23021	9	4.0

ROOM=DCL_CORE_GMCH

PLL SUPPLY FILTER



CAD NOTE:

PLACE THMT CAPS OUTSIDE RM BOUNDARY.
TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL
CAD NOTE: PLACE COMPONENTS AS CLOSE AS POSSIBLE TO
PROCESSOR SOCKET

FILTERED ANALOG SUPPLY

DRAWING

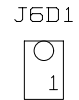
FAB_A.SCH.1.10
Mon Nov 18 13:48:27 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	10	4.0

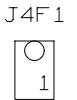
MOD_REV=0.05



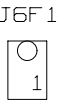
RETENTION ACHOR CLIPS: QTY(4)



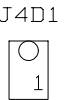
HDR
NB



HDR
NB



HDR
NB



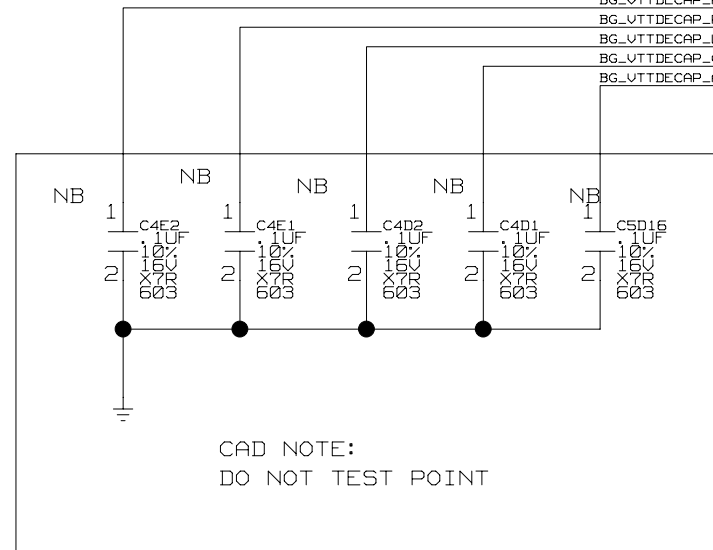
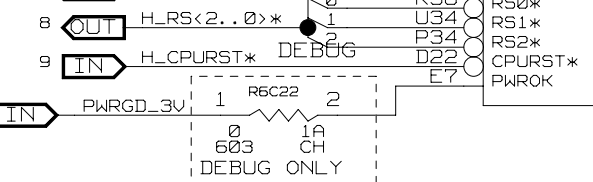
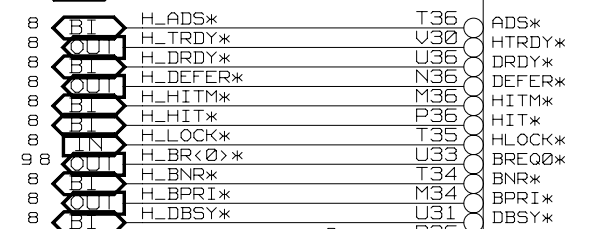
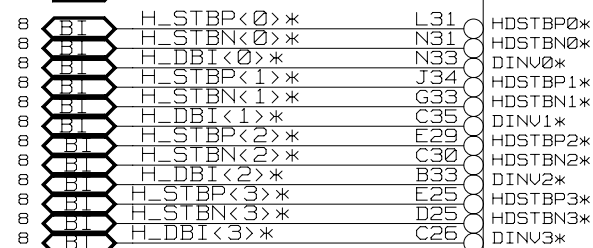
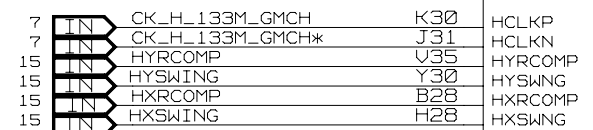
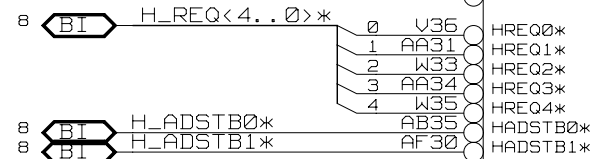
HDB

NB

```
U6D1
G_DDR_2P0
```



3	W3	HA3*	HD0*	T30	0
4	AA33	HA4*	HD1*	R33	1
5	AB30	HA5*	HD2*	R34	2
6	V34	HA6*	HD3*	N34	3
7	Y36	HA7*	HD4*	R31	4
8	AC33	HA8*	HD5*	L33	5
9	Y35	HA9*	HD6*	L36	6
10	AA36	HA10*	HD7*	P35	7
11	AC34	HA11*	HD8*	J36	8
12	AB34	HA12*	HD9*	K34	9
13	Y34	HA13*	HD10*	K36	10
14	AB36	HA14*	HD11*	M30	11
15	AC36	HA15*	HD12*	M35	12
16	AC31	HA16*	HD13*	L34	13
17	AF35	HA17*	HD14*	K35	14
18	AD36	HA18*	HD15*	H36	15
19	AD35	HA19*	HD16*	G34	16
20	AE34	HA20*	HD17*	G36	17
21	AD34	HA21*	HD18*	J33	18
22	AE36	HA22*	HD19*	D35	19
23	AF36	HA23*	HD20*	F36	20
24	AE33	HA24*	HD21*	F34	21
25	AF34	HA25*	HD22*	E36	22
26	AG34	HA26*	HD23*	H34	23
27	AG36	HA27*	HD24*	F35	24
28	AE31	HA28*	HD25*	D36	25
29	AH35	HA29*	HD26*	H35	26
30	AG33	HA30*	HD27*	E33	27
31	AG31	HA31*	HD28*	E34	28



CAD NOTE:
DO NOT TEST POINT

U6D1 BDG_DDR_2P0

ROOM=DCL_00

V_1P5_CORE

VCCA_DPLL

V_1P5_DAC

V_1P5_VCCA_FSB

V_1P5_CORE

V_1P5_VCCA_SM

V_2P5_VCCQ

V_2P5_SM

VCCP

VCC3

DRAWING

FAB_A.

Mon Nov 18 13:48:3

D845GFT FAB_A

3 OF 5

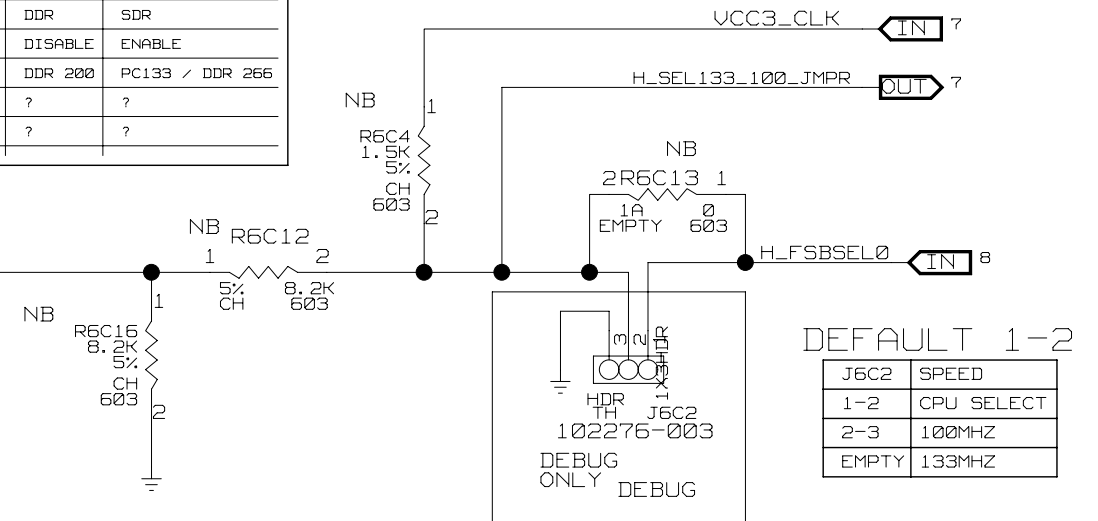
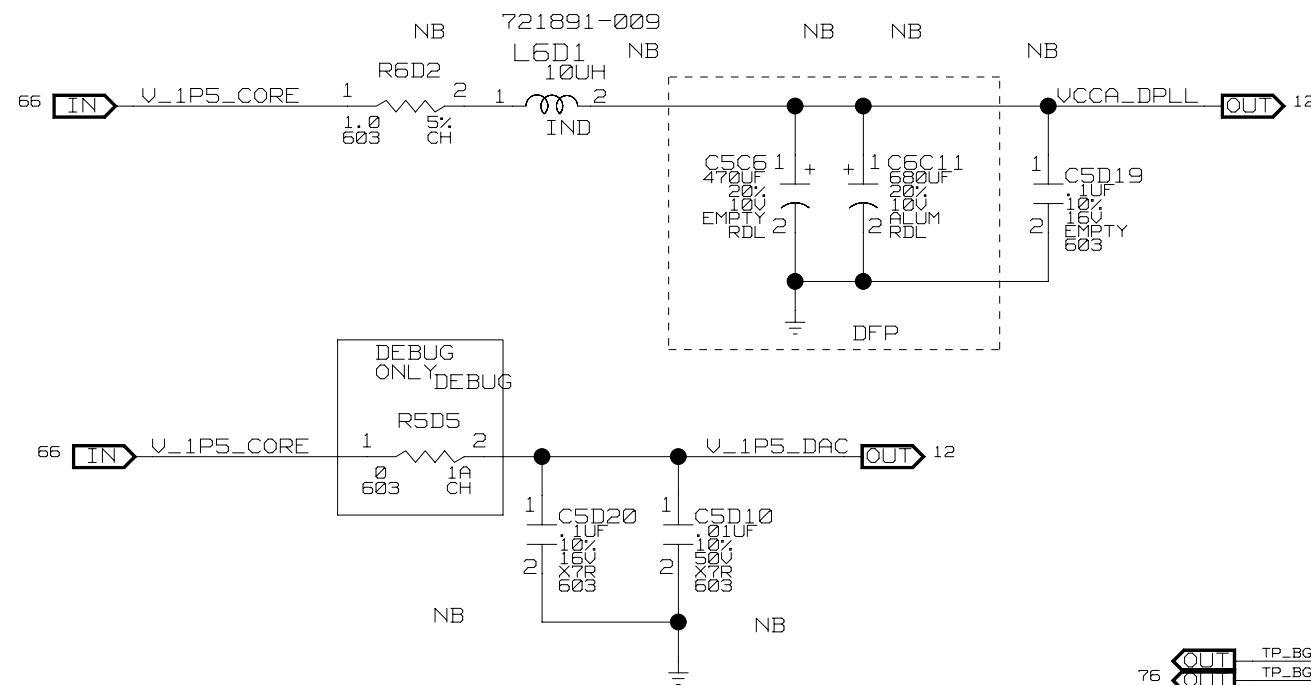
IC

DOCUMENT NUMBER

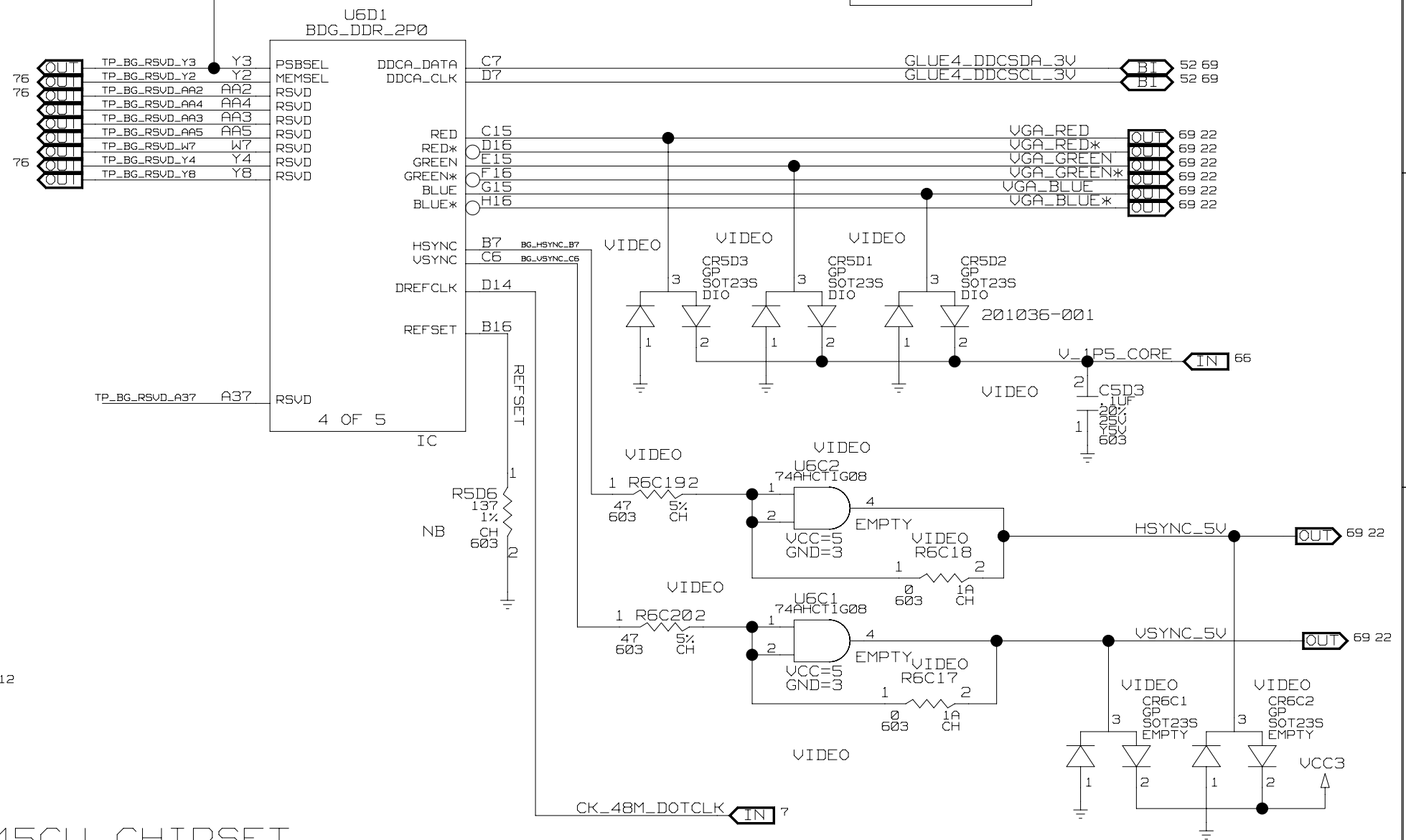
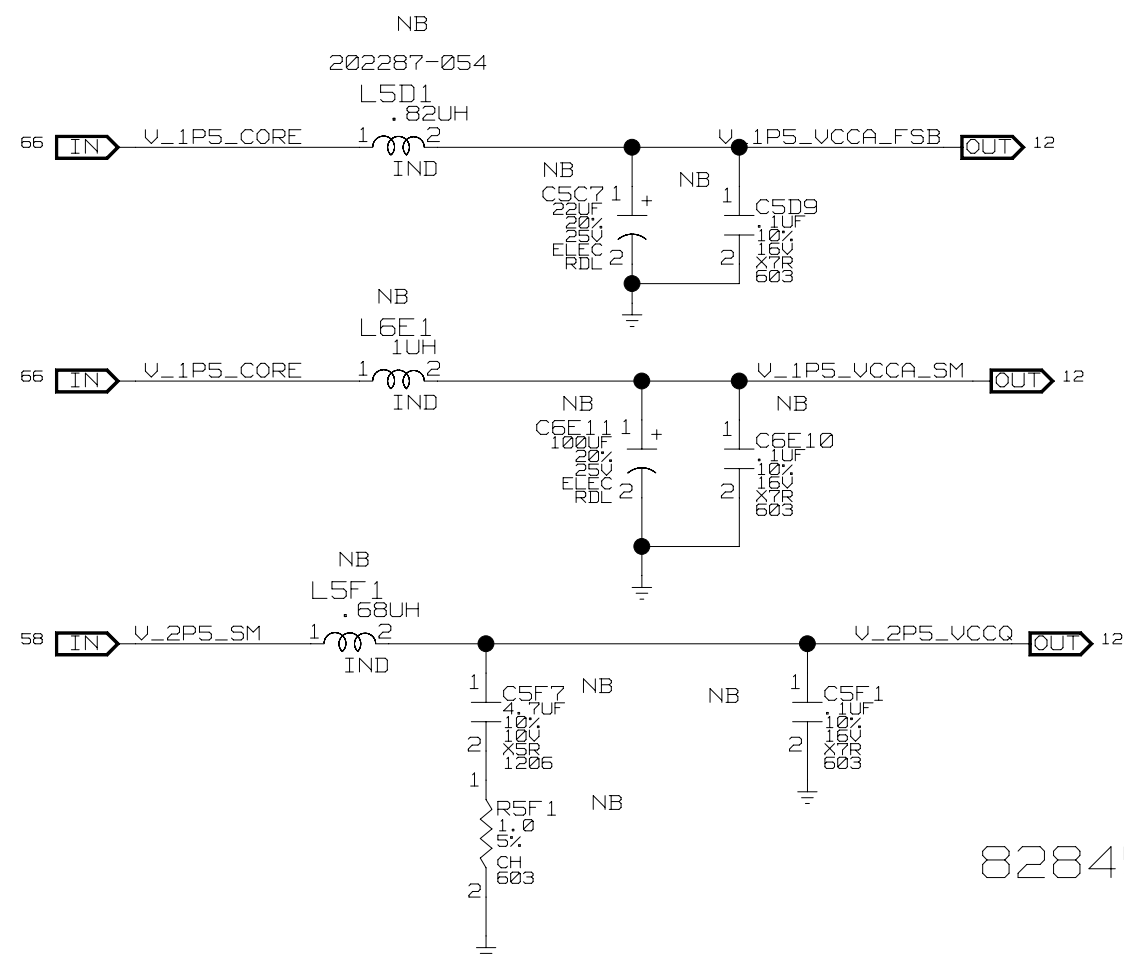
DRAWING FAB_A.SCH.1.12
Mon Nov 18 13:48:37 2002
D845GFT FAB_A

ROOM=DCL_CORE_GMCH

PILOT	BALL	FUNCTION	H	L
0	Y3	FSB SPEED	133	100
1	Y2	MEMORY TYPE	DDR	SDR
2	AA2	INT. GFX DIS	DISABLE	ENABLE
3	Y4	MEMORY SPEED	DDR 200	PC133 / DDR 266
4	AA3	RSURD	?	?
5	AA5	RSURD	?	?



ANALOG FILTERS



82845GV CHIPSET
PART 3 OF 3

D845GFT FAB_A
DRAWING FAB_A.SCH. 1.13
Mon Nov 18 13:48:47 2002

DOCUMENT NUMBER	PAGE	REV
C23021	13	4.0

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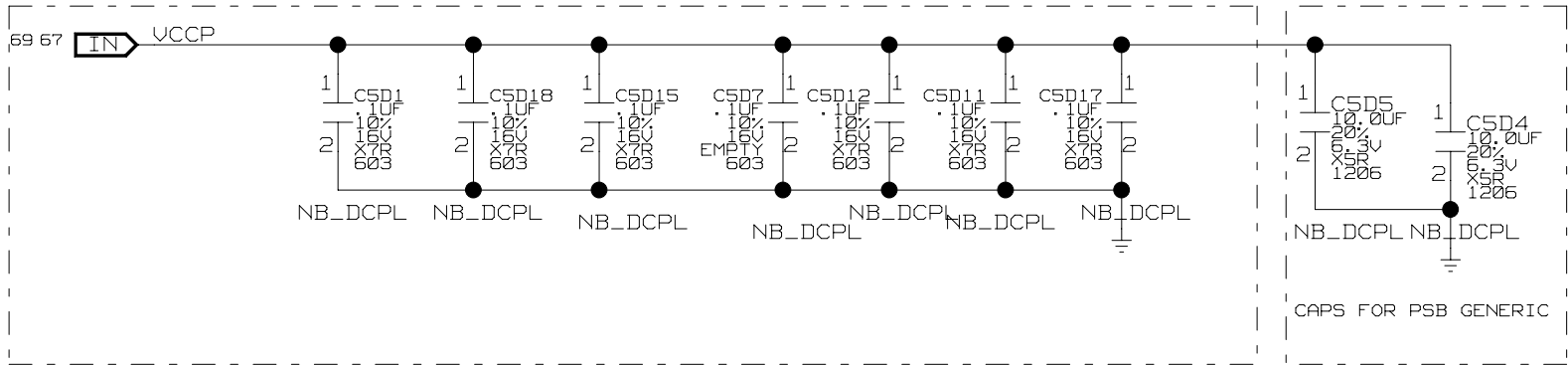
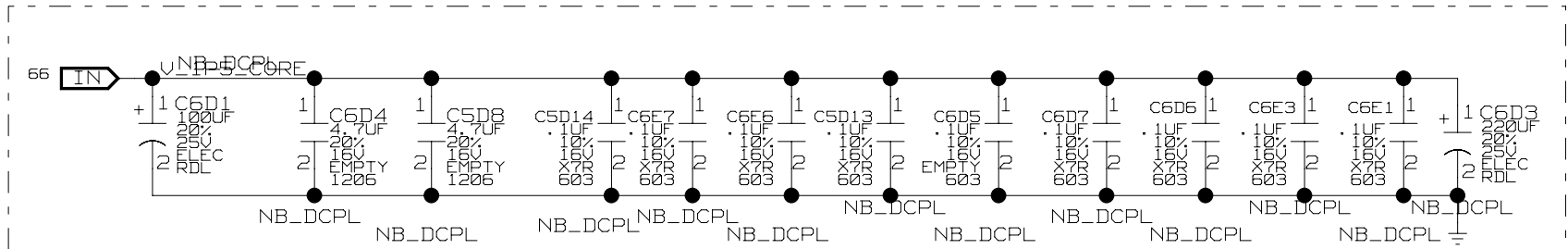
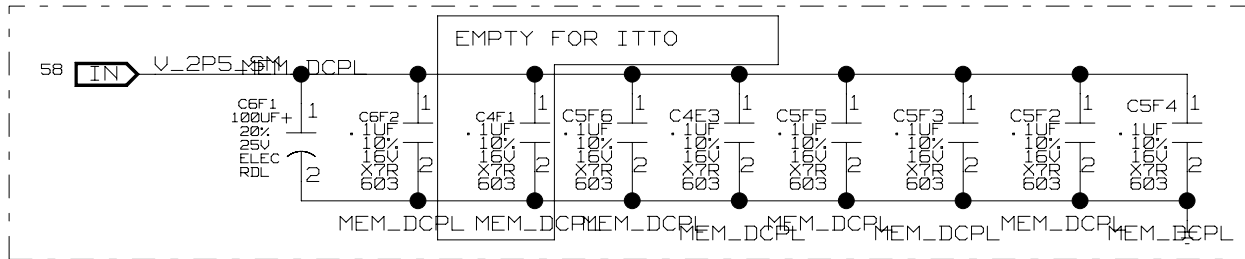
DRAWING

Mon Nov 25 12:48:57 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	14	4.0

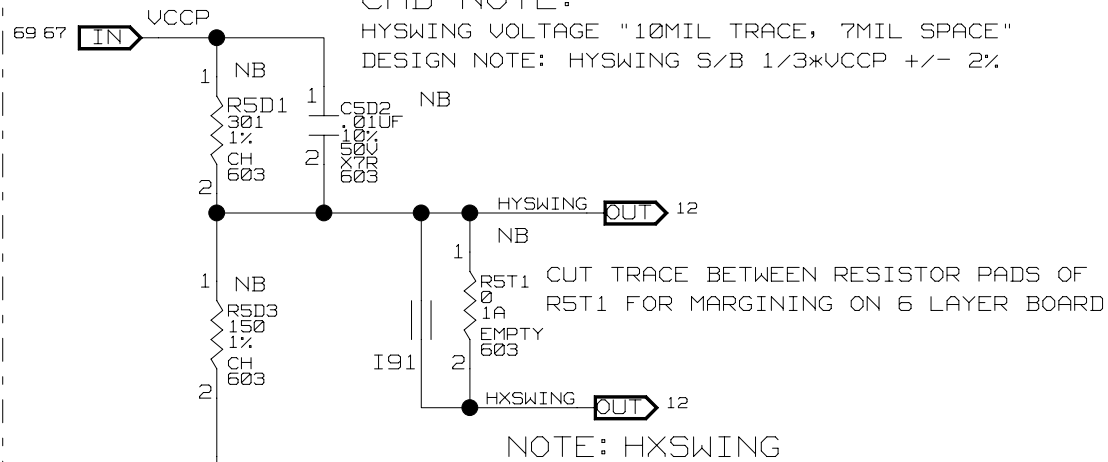
ROOM=DCL_CORE_GMCH

SYSTEM MEMORY DECOUPLING

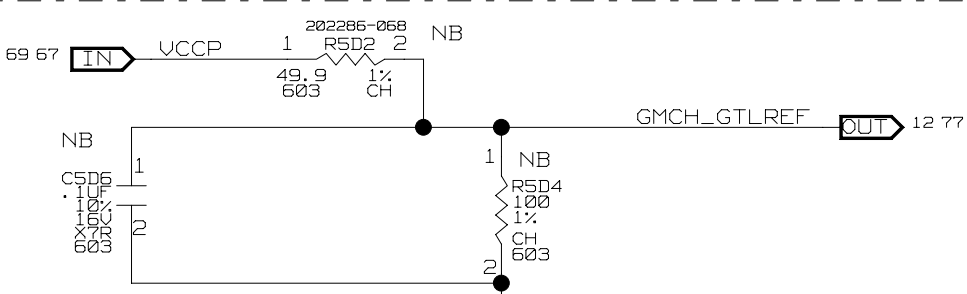


CAD NOTE:

HYSWING VOLTAGE "10MIL TRACE, 7MIL SPACE"
DESIGN NOTE: HYSWING S/B 1/3*VCCP +/- 2%



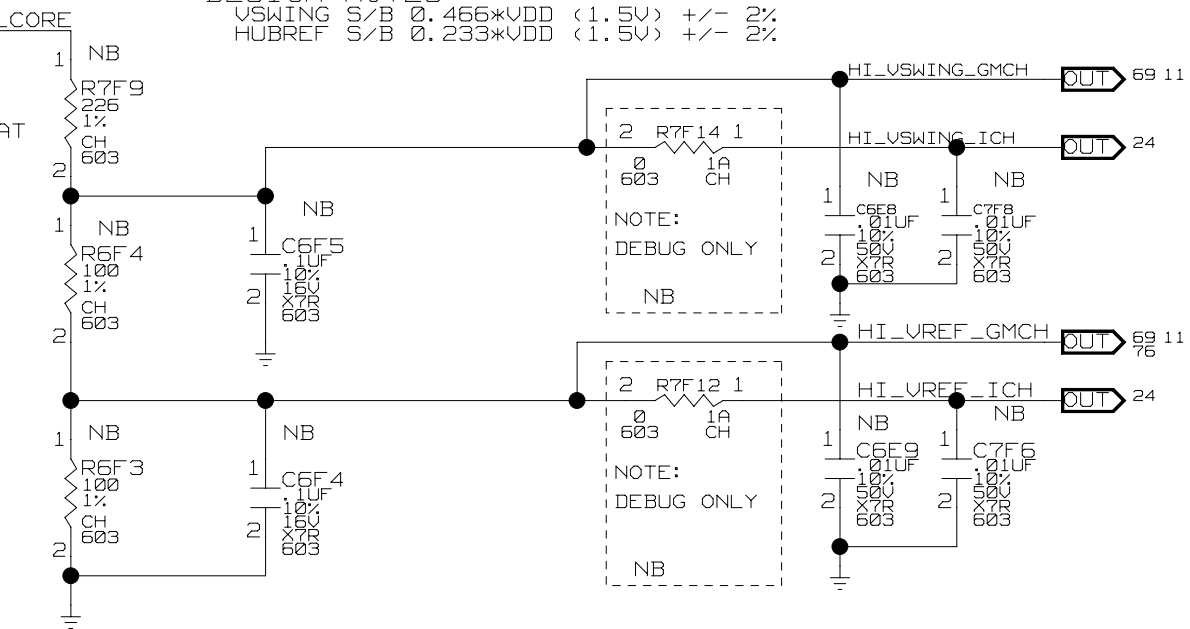
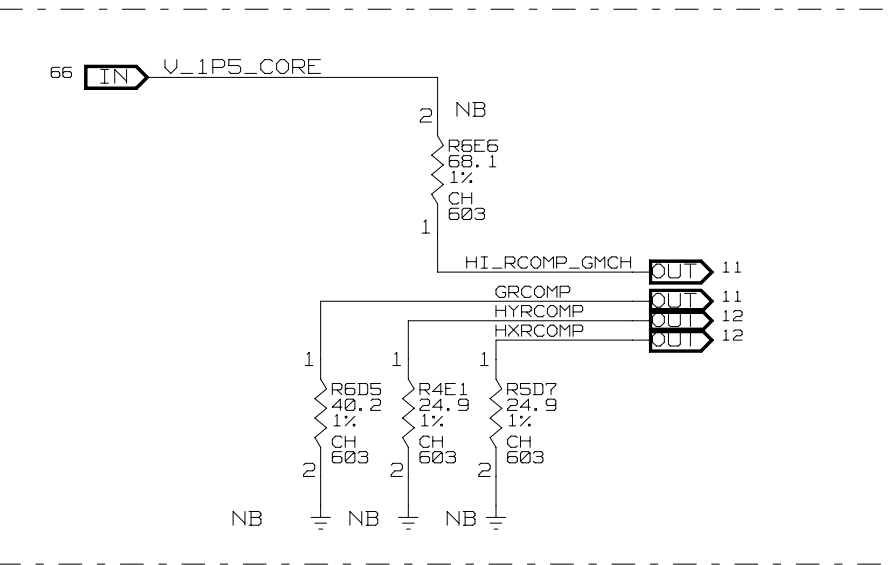
NOTE: HXSWING



DESIGN NOTES:

VSWING S/B 0.466*VDD (1.5V) +/- 2%
HUBREF S/B 0.233*VDD (1.5V) +/- 2%

PLACEMENT NOTES:
RESISTOR DIVIDER PLUS 1 CAP PLACED AT MIDPOINT OF BUS. TWO OTHER CAPS PLACED 1 EA AT GMCH AND ICH
USE 10MIL TRACE, ISOLATE W/ 7MIL SPACE



CHIPSET DECOUPLING, STRAPPING

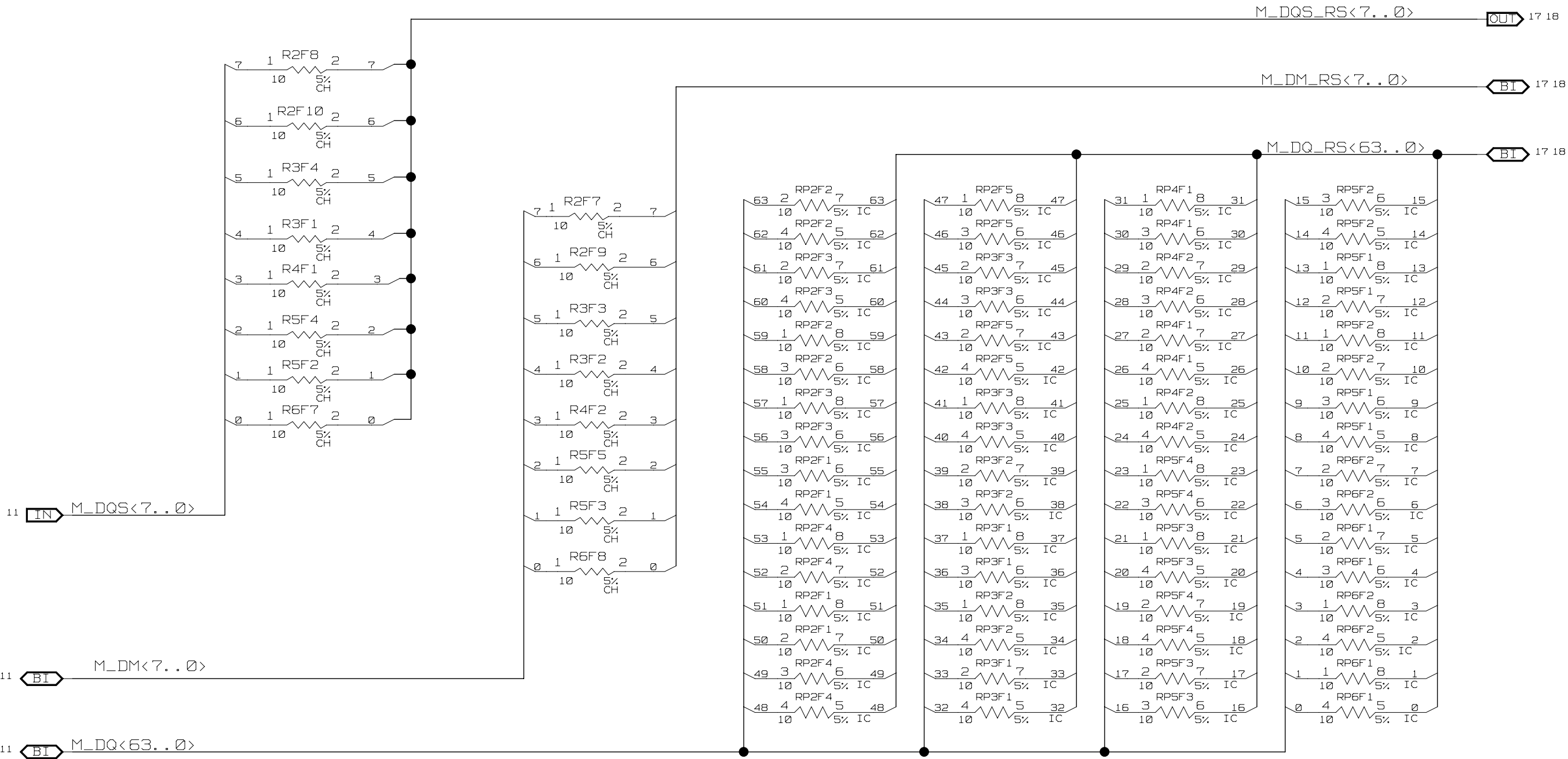
DRAWING

FAB_A.SCH.1.15
Mon Nov 18 13:48:55 2002
D845GFT FAB_A

DOCUMENT NUMBER
C23021
PAGE
15
REV
4.0

DDR SERIES RESISTORS

ROOM=DCL_DDR_CORE



ROOM=DCL_DDR_CORE

DDR TERMINATION RESISTORS

59INV_1P25_MEMUTT

M_DQS_RS<7..0>

M_DM_RS<7..0>

M_DQ_RS<63..0>

M_MAA<12..0>

[PAGE_TITLE=DDR_TERMINATION_RESISTORS]

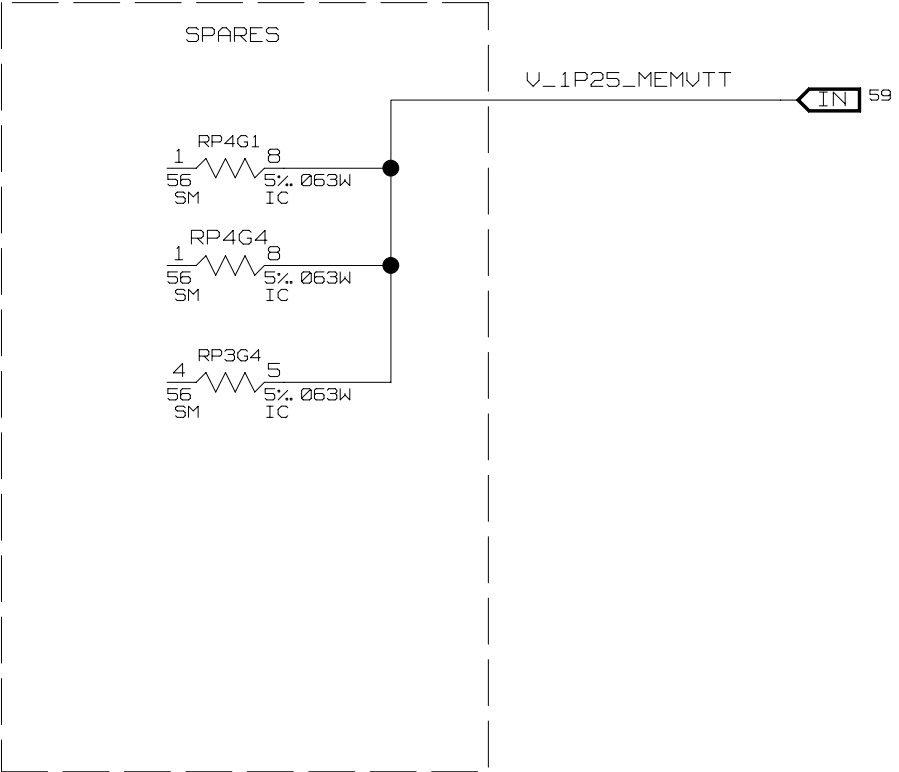
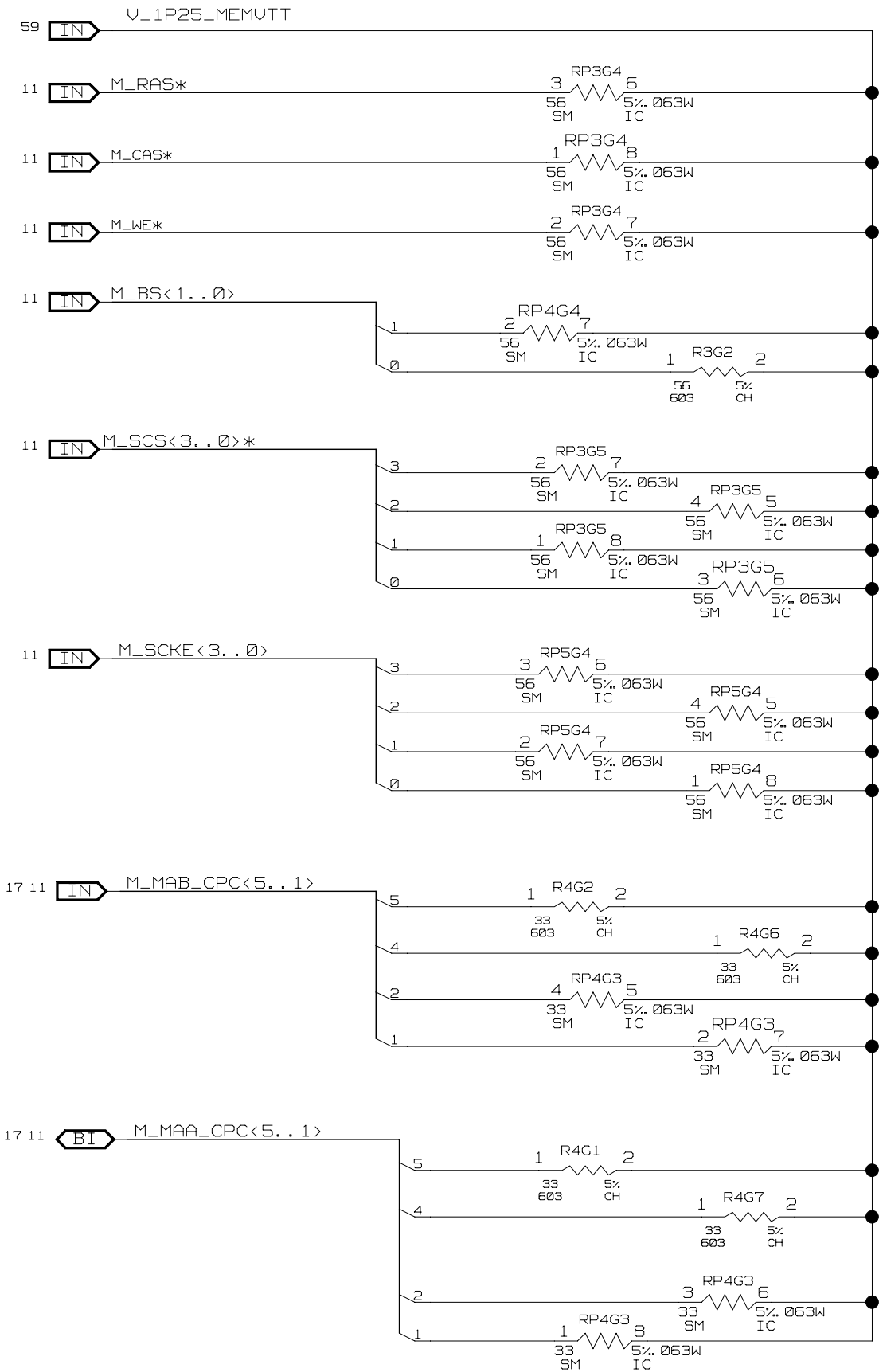
DRAWING

FAB_A.SCH.1.18
Mon Nov 18 12:44:14 2002
0845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	18	4.0

ROOM=DCL_DDR_CORE

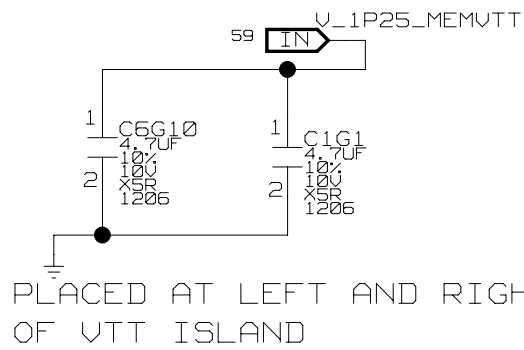
DDR TERMINATION RESISTORS



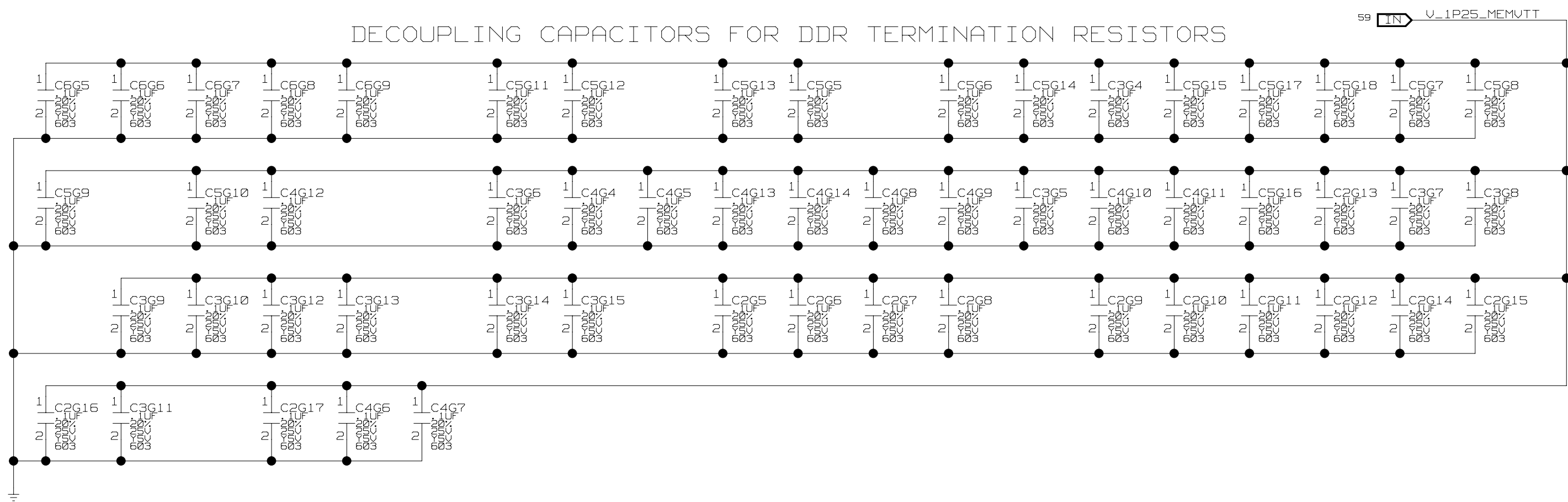
NOTE:
CS SIGNALS MUST HAVE IT'S OWN RES/RPACK
CKE SIGNALS MUST HAVE IT'S OWN RES/RPACK
CPC SIGNALS MUST HAVE IT'S OWN RES/RPACK

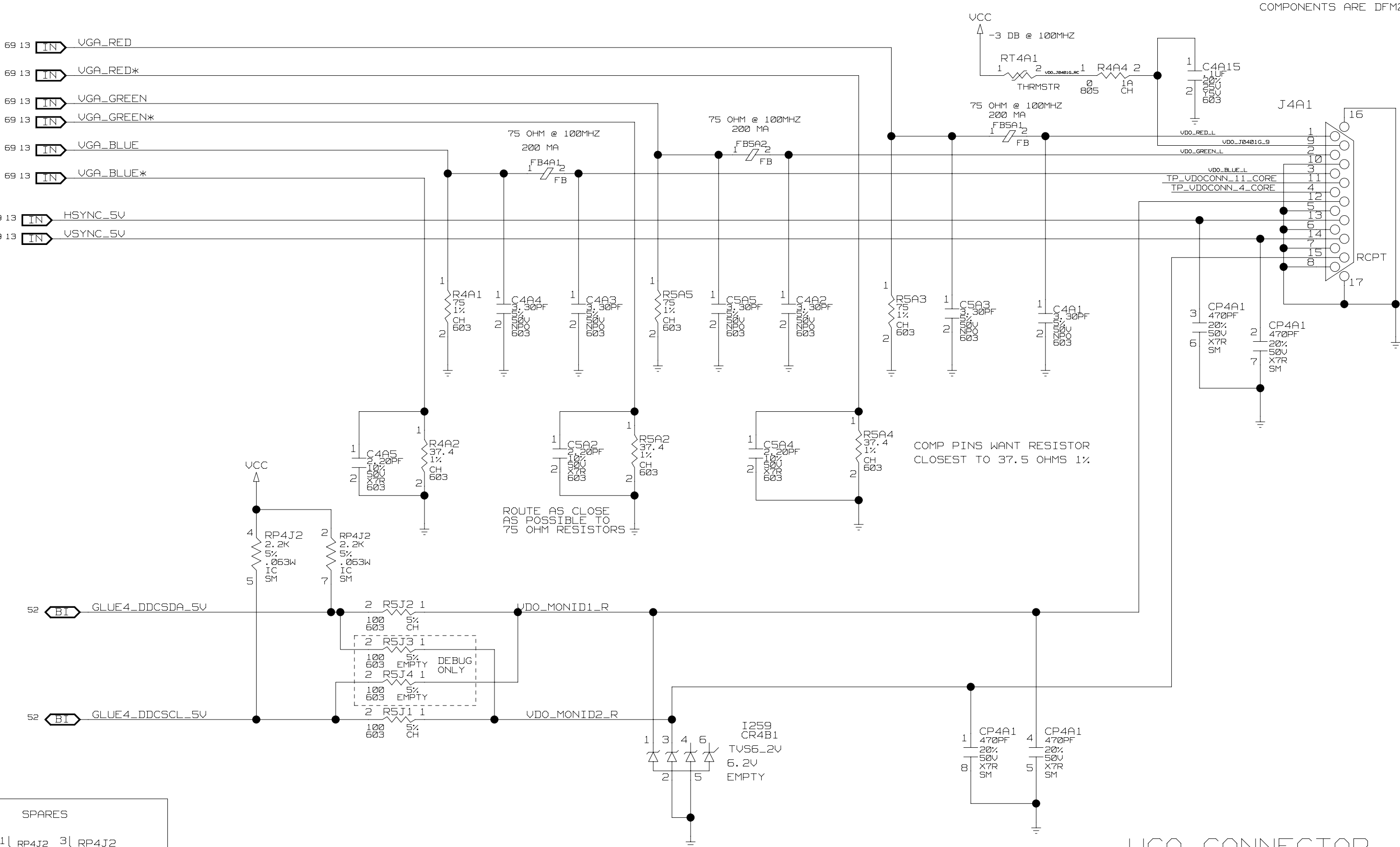
DRAWING FAB_A.SCH.1.19
Mon Nov 18 12:44:23 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	19	4.0

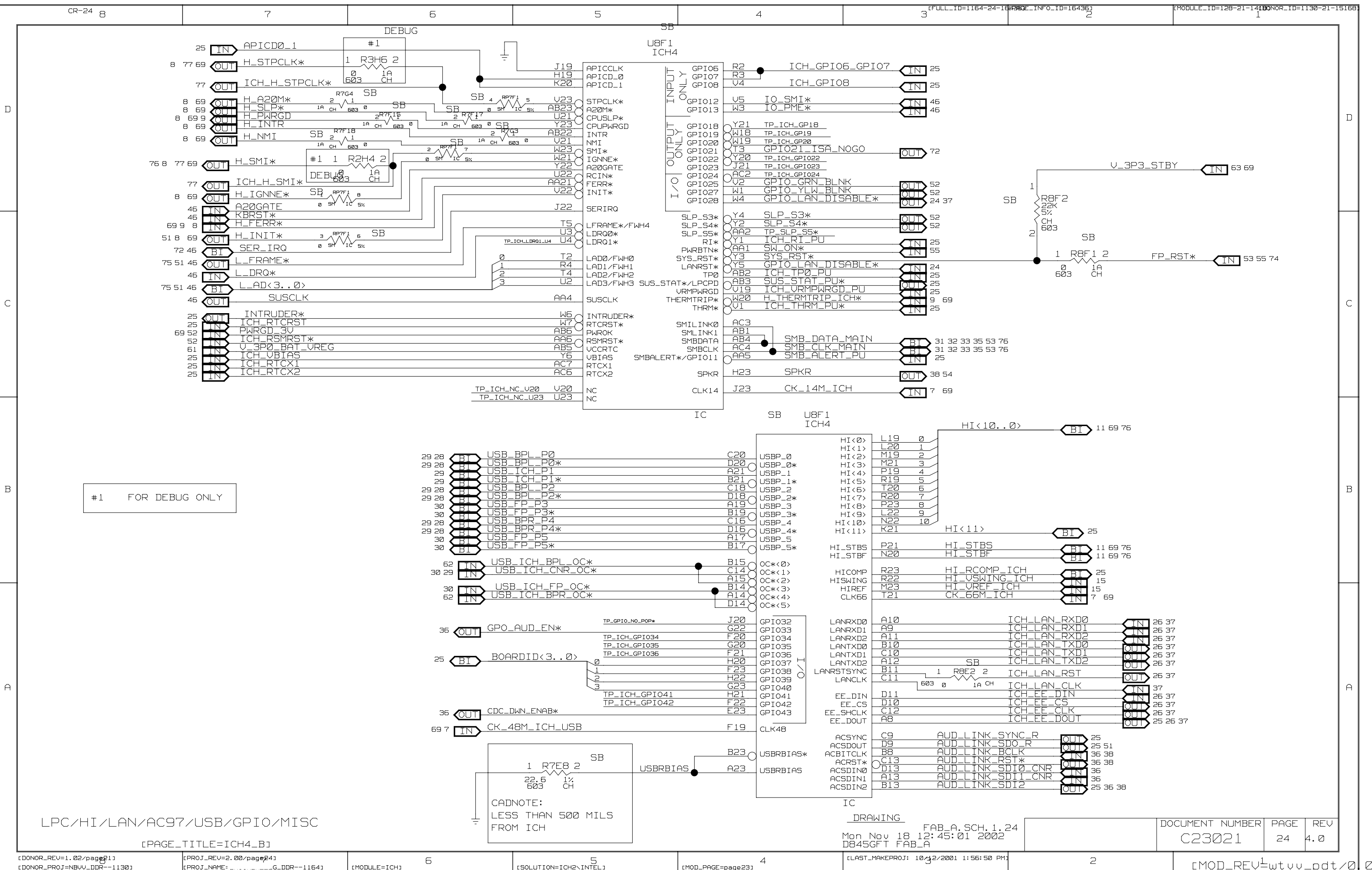


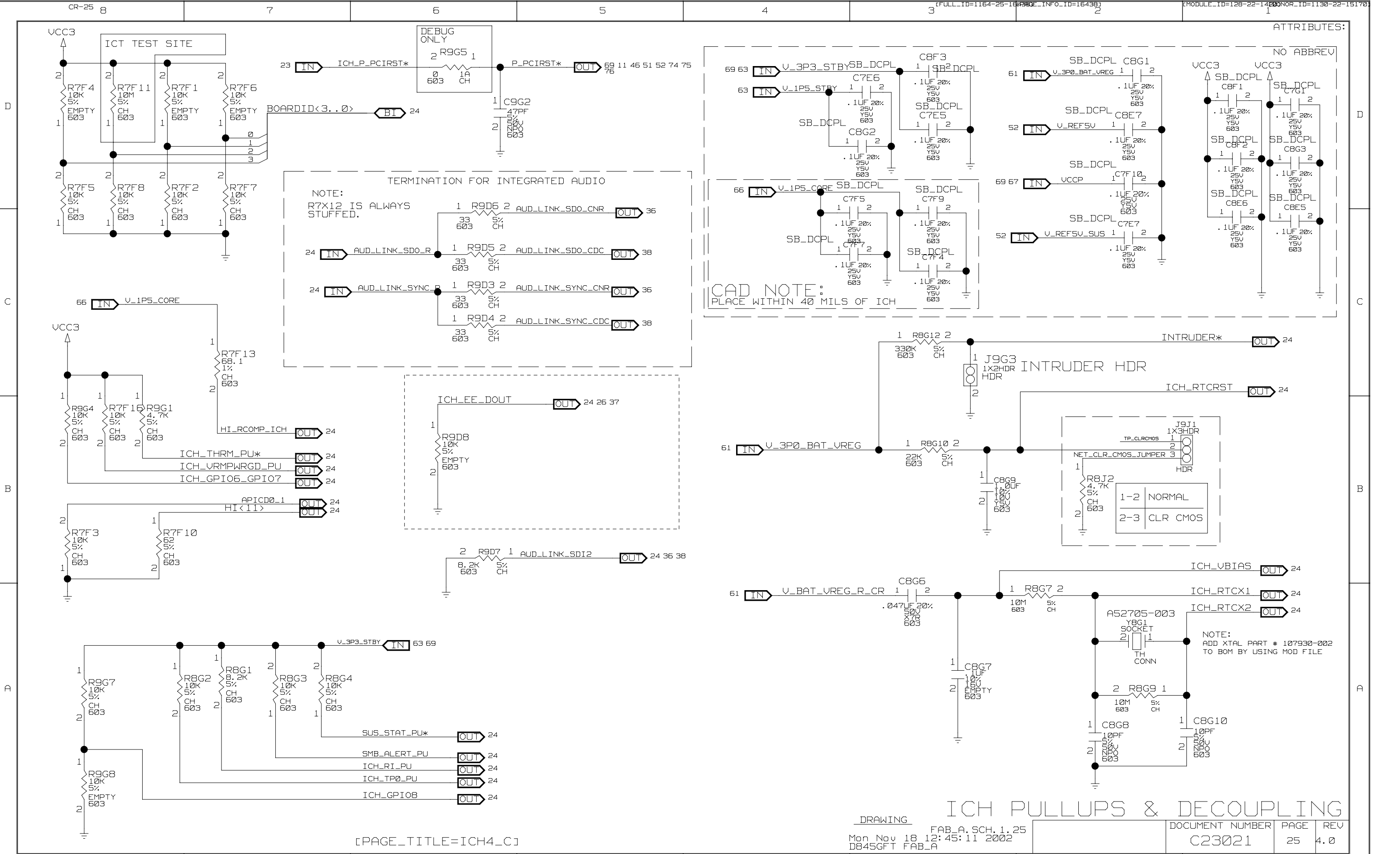
DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS





VGA CONNECTOR

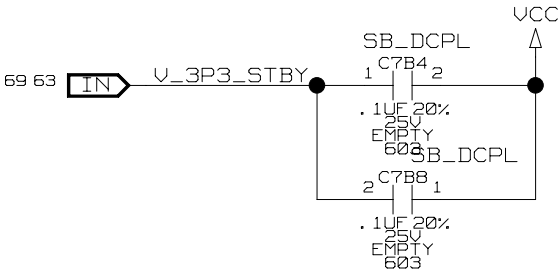
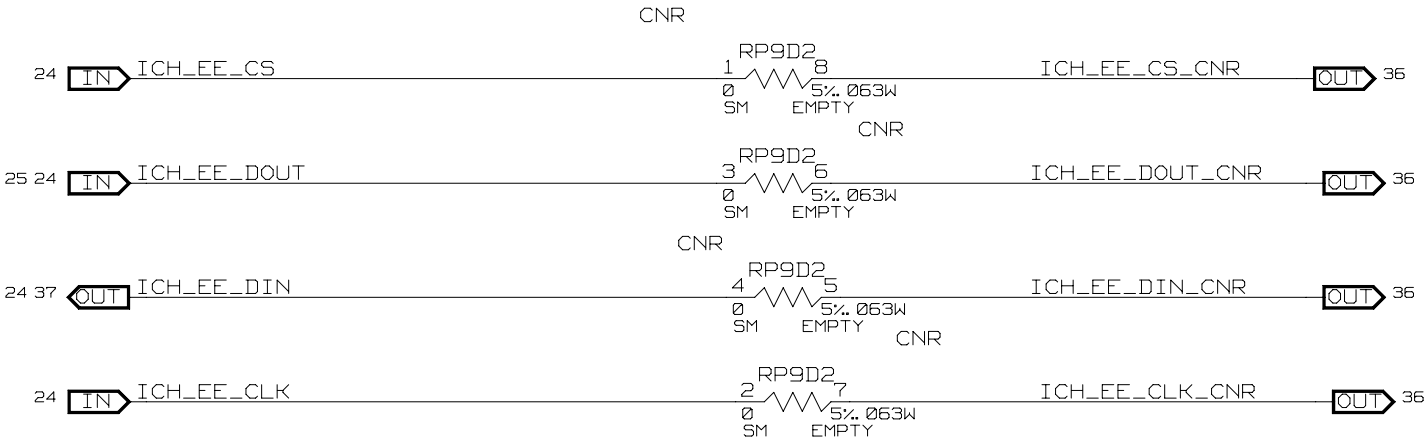
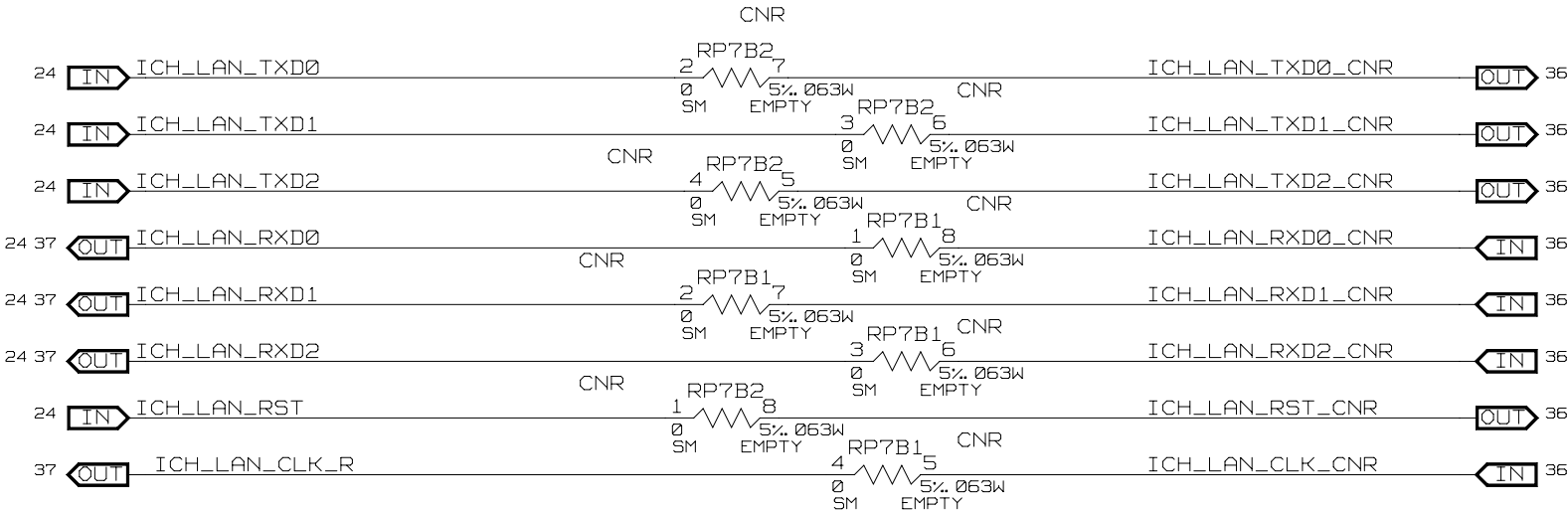




ICH AND CNR LINK STUFFING OPTION PAGE

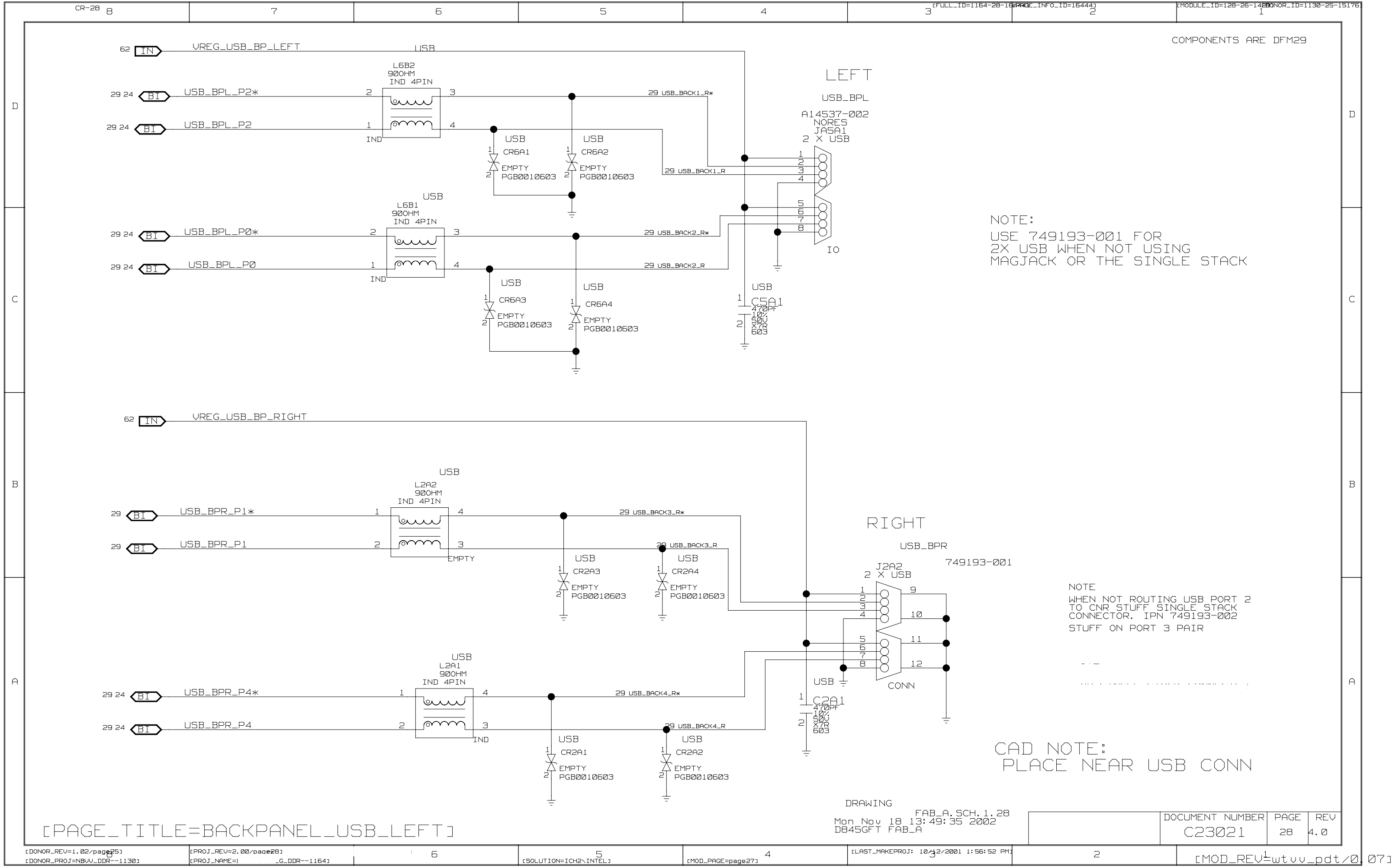
CAD NOTE:
PLACE THESE R-PACKS UNDERNEATH
THE LAN CHIP, RIGHT BY THE PINS TO
MINIMIZE STUB FROM PIN TO R-PACK

STUFF ONLY WHEN YOU HAVE CNR AND NO LAN.

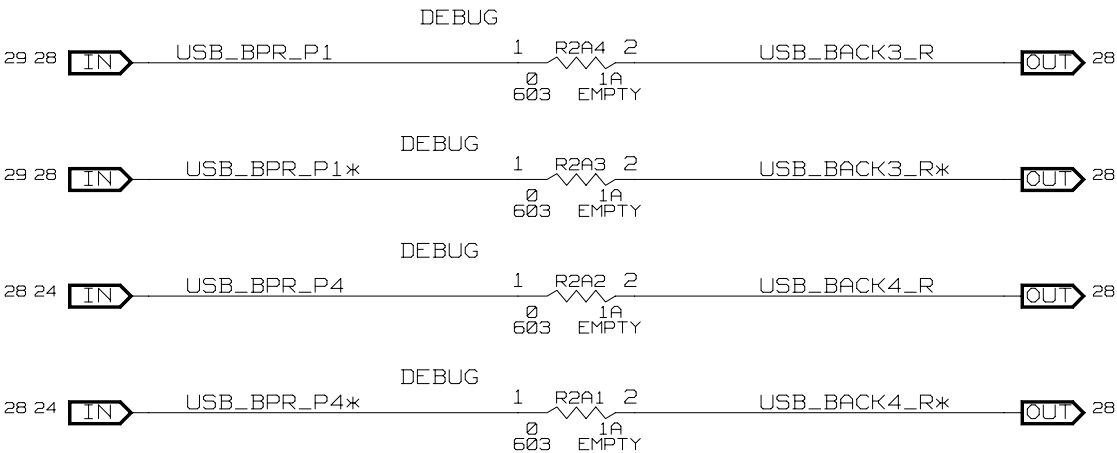
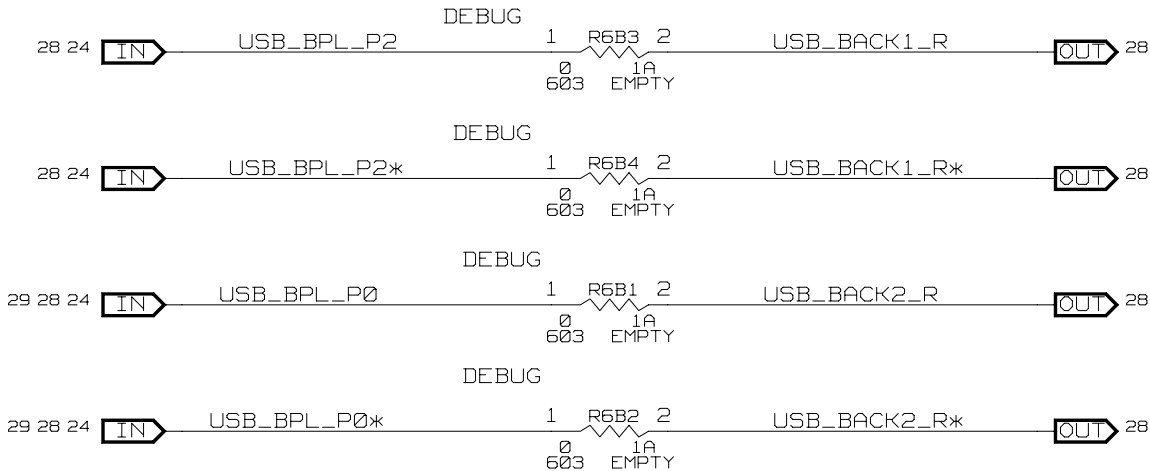
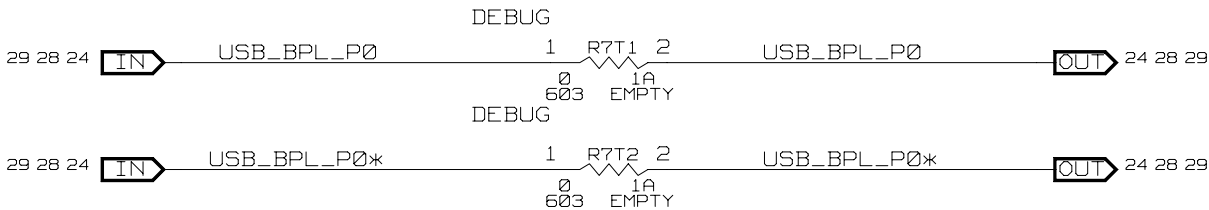
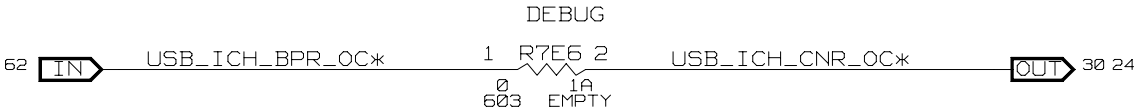
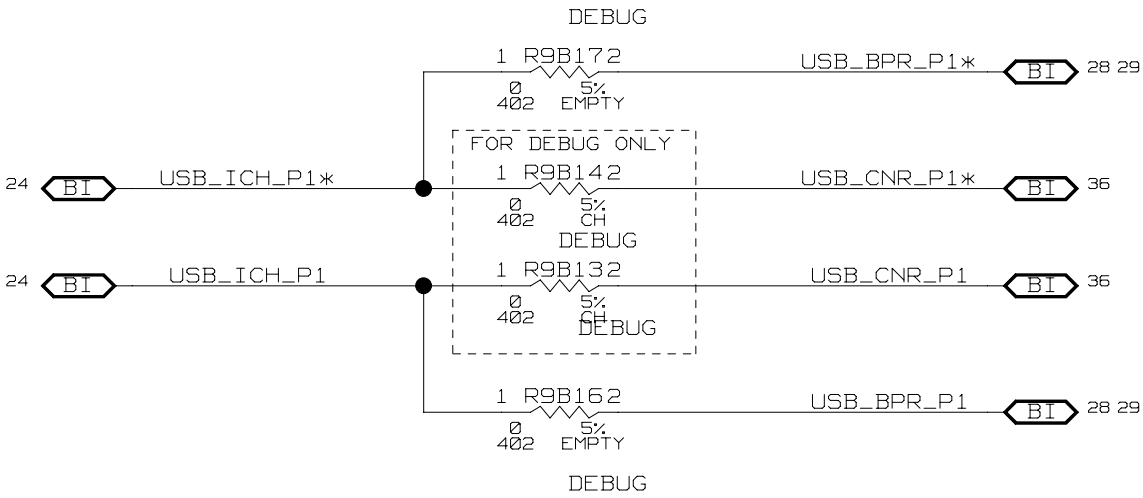


0-OHMS ARE PROVIDED
TO MINIMIZE STUBS
ON LAN INTERFACE

[PAGE_TITLE=ICH_360]



NOTE:
STUFF THESE 3 RESISTORS WHEN SUPPORTING 4 USB PORTS
OUT THE BACKPANEL AND NO CNR CONNECTOR.



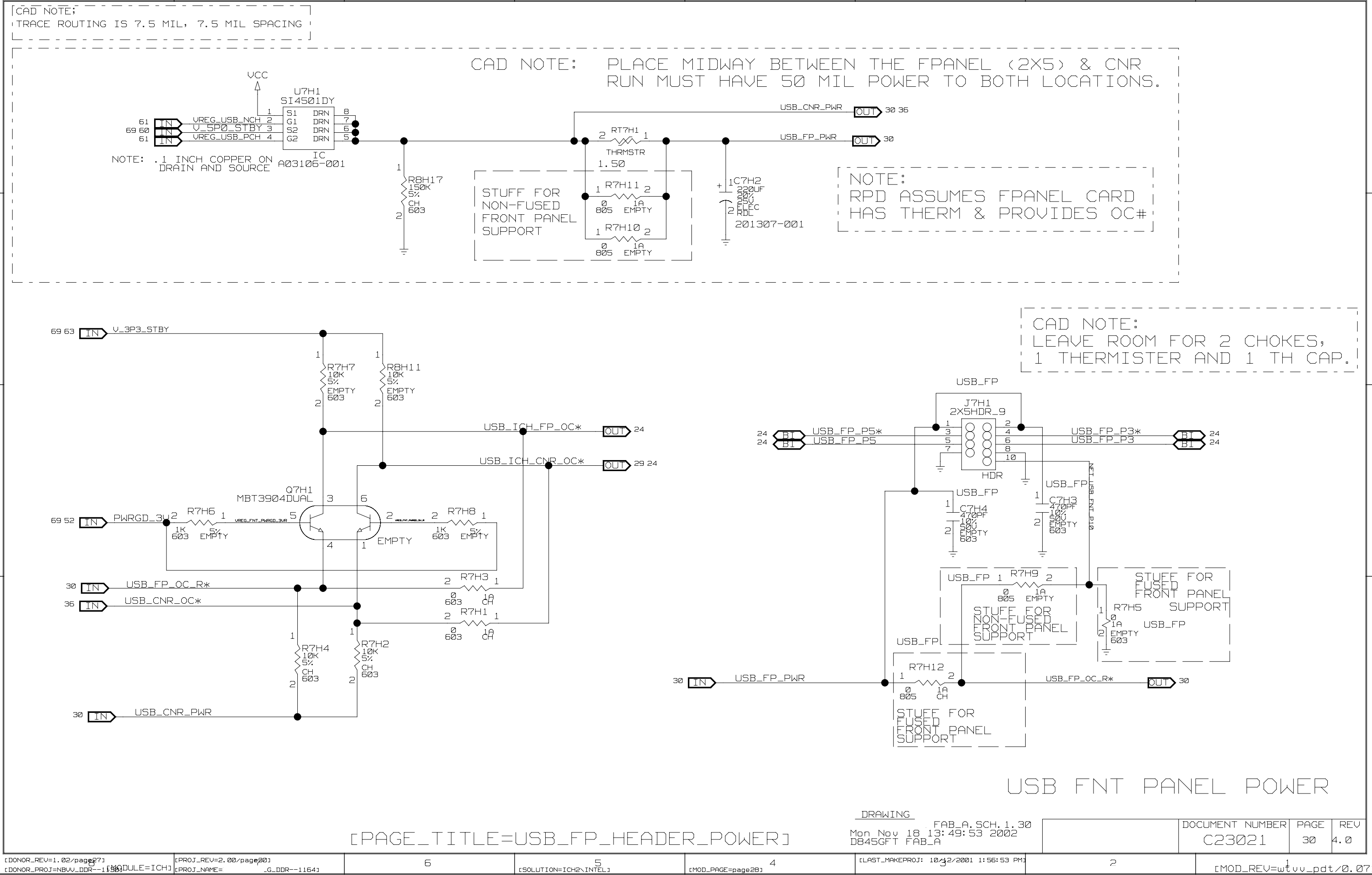
NOTE:
FOR DEBUG ONLY

[PAGE_TITLE=BLANK]

DRAWING

FAB_A.SCH.1.29
Mon Nov 18 13:49:44 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	29	4.0



D

D

C

C

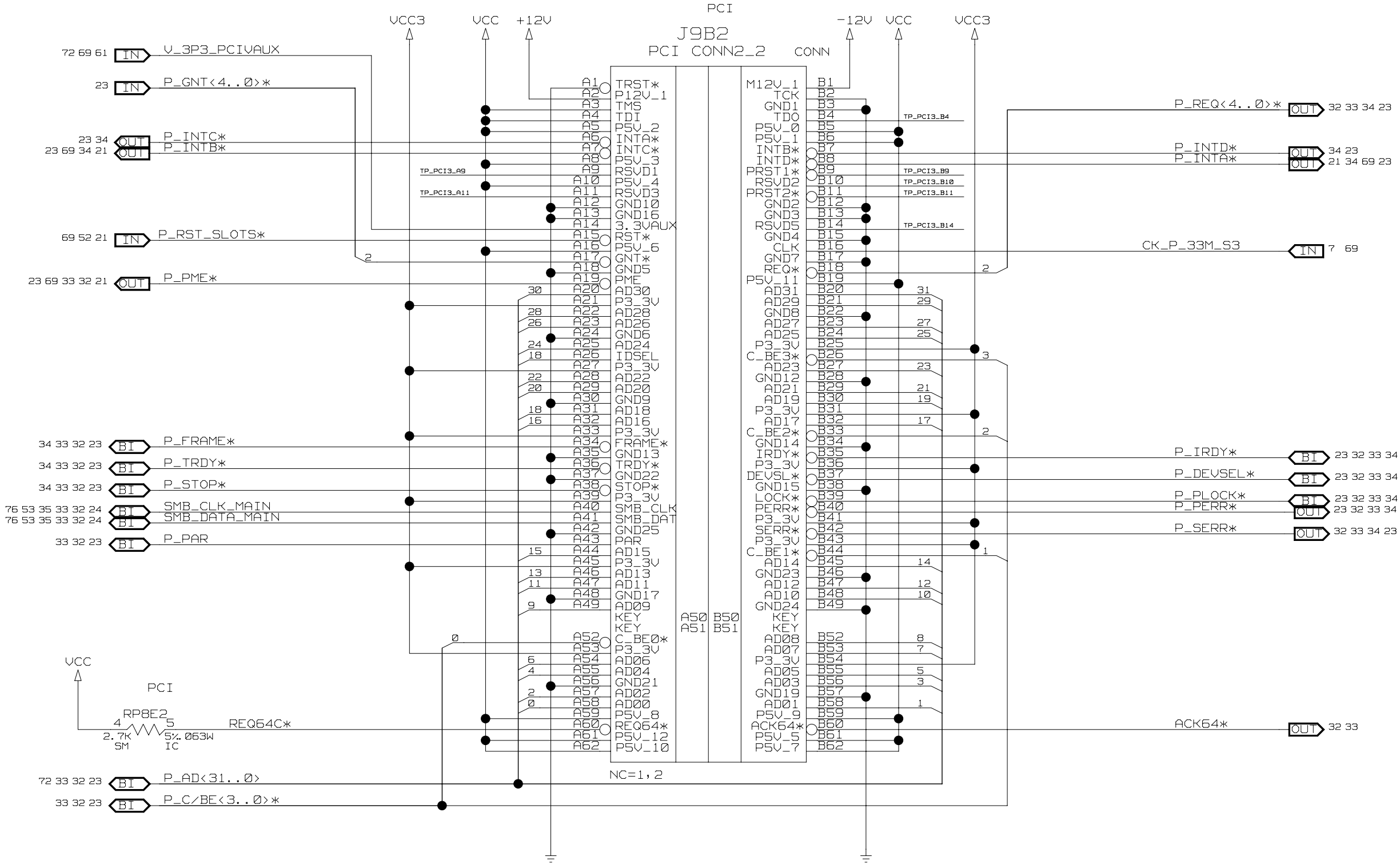
B

B

A

A

PCI SLOT 3



DESIGN NOTE:
PCI SLOT3 = PCI DEVICE #18
REQ/GNT PAIR = #2
IRQ MAP A : B : C : D
 C : D : B : A

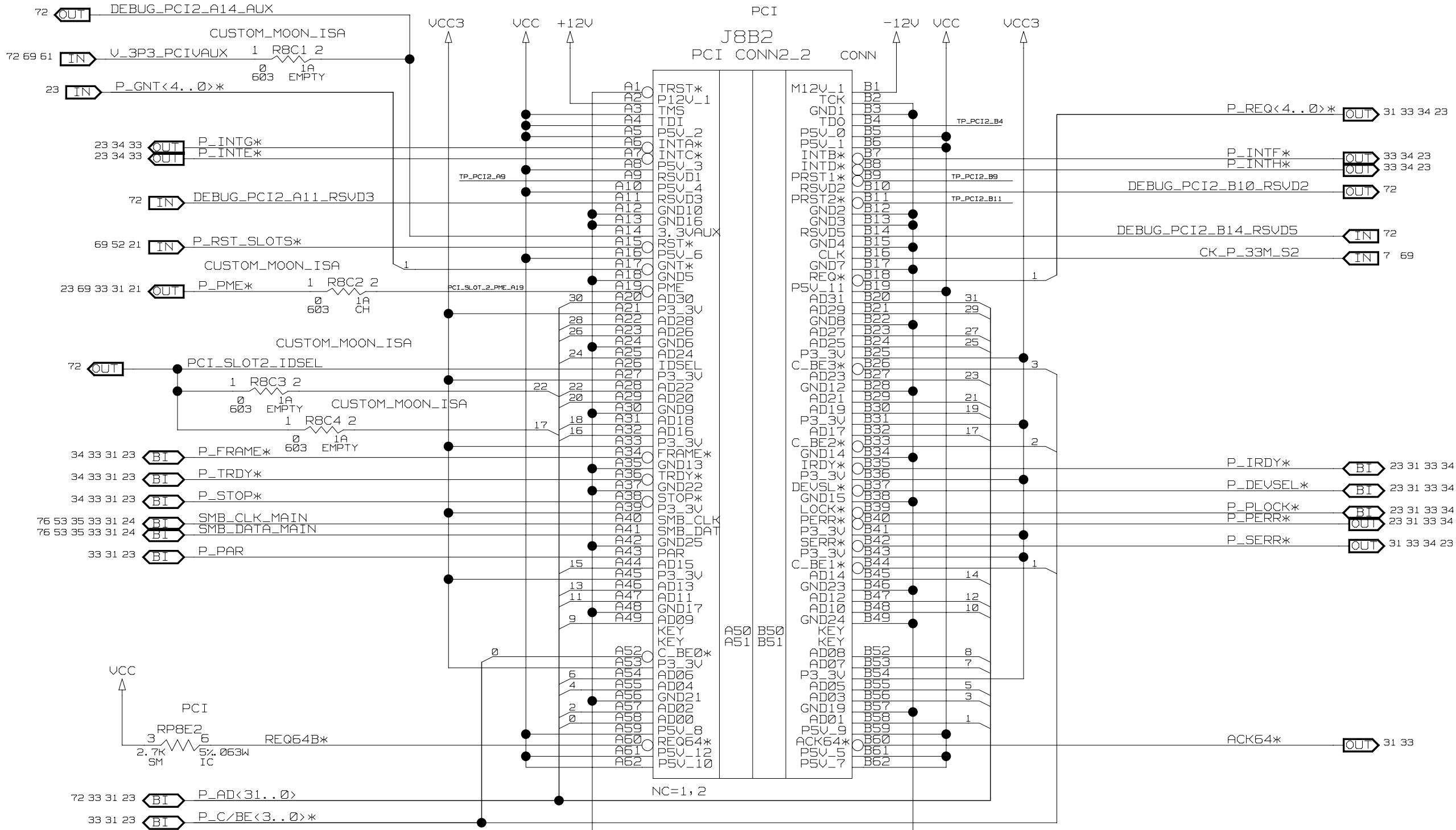
PCI SLOT 3

[PAGE_TITLE=PCI_SLOT3]

DRAWING
FAB_A.SCH.1.31
Mon Nov 18 13:50:03 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	31	4.0

PCI SLOT 2



DESIGN NOTE:

PCI SLOT2 = PCI DEVICE #17/22
REQ/GNT PAIR = #1
IRQ MAP A : B : C : D
G : F : E : H

[PAGE_TITLE=PCI_SLOT2]

DRAWING

FAB_A.SCH.1.32
Mon Nov 18 13:50:14 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	32	4.0

D

C

B

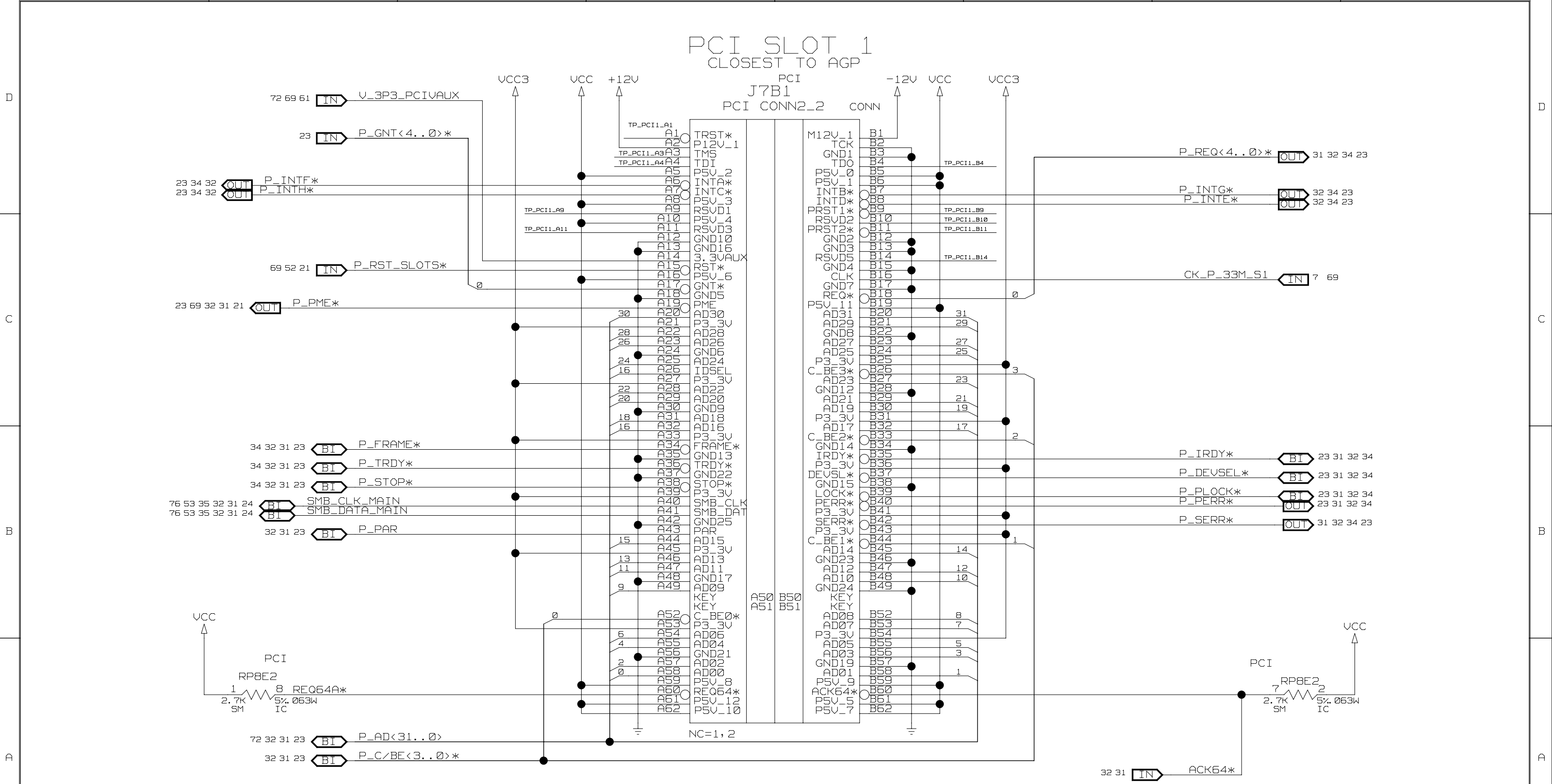
A

D

C

B

A



M12V_1

B1

TCK

GND1

B2

GND1

TDO

B3

TDO

P5V_0

B4

P5V_0

P5V_1

B5

P5V_1

INTB*

B6

INTB*

INTD*

B7

INTD*

PRST1*

B8

PRST1*

RSVD2

B9

RSVD2

PRST2*

B10

PRST2*

GND2

B11

GND2

GND3

B12

GND3

RSVD5

B13

RSVD5

GND4

B14

GND4

CLK

B15

CLK

GND7

B16

GND7

REQ*

B17

REQ*

P5V_11

B18

P5V_11

AD31

B19

AD31

AD29

B20

AD29

GND8

B21

GND8

AD27

B22

AD27

AD25

B23

AD25

P3_3V

B24

P3_3V

C_BE3*

B25

C_BE3*

AD23

B26

AD23

GND12

B27

GND12

AD21

B28

AD21

AD19

B29

AD19

P3_3V

B30

P3_3V

AD17

B31

AD17

C_BE2*

B32

C_BE2*

GND14

B33

GND14

IRDY*

B34

IRDY*

P3_3V

B35

P3_3V

DEVSL*

B36

DEVSL*

GND15

B37

GND15

LOCK*

B38

LOCK*

PERR*

B39

PERR*

P3_3V

B40

P3_3V

SERR*

B41

SERR*

P3_3V

B42

P3_3V

C_BE1*

B43

C_BE1*

AD14

B44

AD14

GND23

B45

GND23

AD12

B46

AD12

AD10

B47

AD10

GND24

B48

GND24

KEY

B49

KEY

AD08

B50

AD08

AD07

B51

AD07

P3_3V

B52

P3_3V

AD05

B53

AD05

AD03

B54

AD03

GND19

B55

GND19

AD01

B56

AD01

P5V_9

B57

P5V_9

ACK64*

B58

ACK64*

P5V_5

B59

P5V_5

P5V_7

B60

P5V_7

P5V_7

B61

P5V_7

P5V_7

B62

P5V_7

P_REQ<4..0>*

OUT

31 32 34 23

P_INTG*

OUT

32 34 23

P_INTE*

OUT

32 34 23

CK_P_33M_S1

IN

7 69

P_IRDY*

BI

23 31 32 34

P_DEVSEL*

BI

23 31 32 34

P_PLOCK*

BI

23 31 32 34

P_PERR*

OUT

23 31 32 34

P_SERR*

OUT

31 32 34 23

ACK64*

IN

32 31

PCI

RP8E2

1

2.7k

SM

8

REQ64A*

5% .063W

IC

PCI

RP8E2

7

2.7k

SM

2

5% .063W

IC

VCC3

VCC

+12V

-12V

VCC

VCC3

VCC

VCC

DESIGN NOTE:

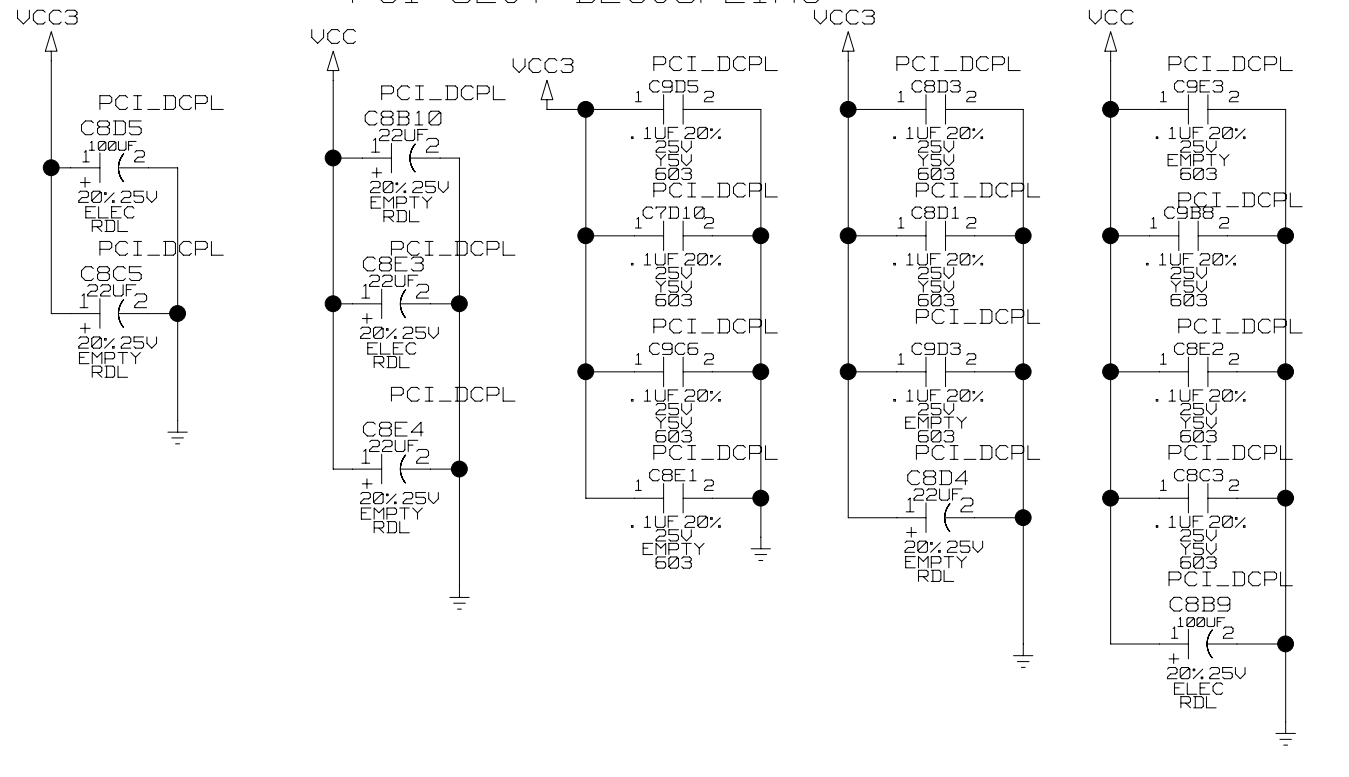
PCI SLOT1 = PCI DEVICE #16
REQ/GNT PAIR = #0
IRQ MAP A : B : C : D
F : G : H : E

DRAWING

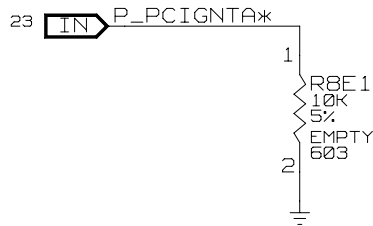
FAB_A.SCH.1.33
Mon Nov 18 13:50:24 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	33	4.0

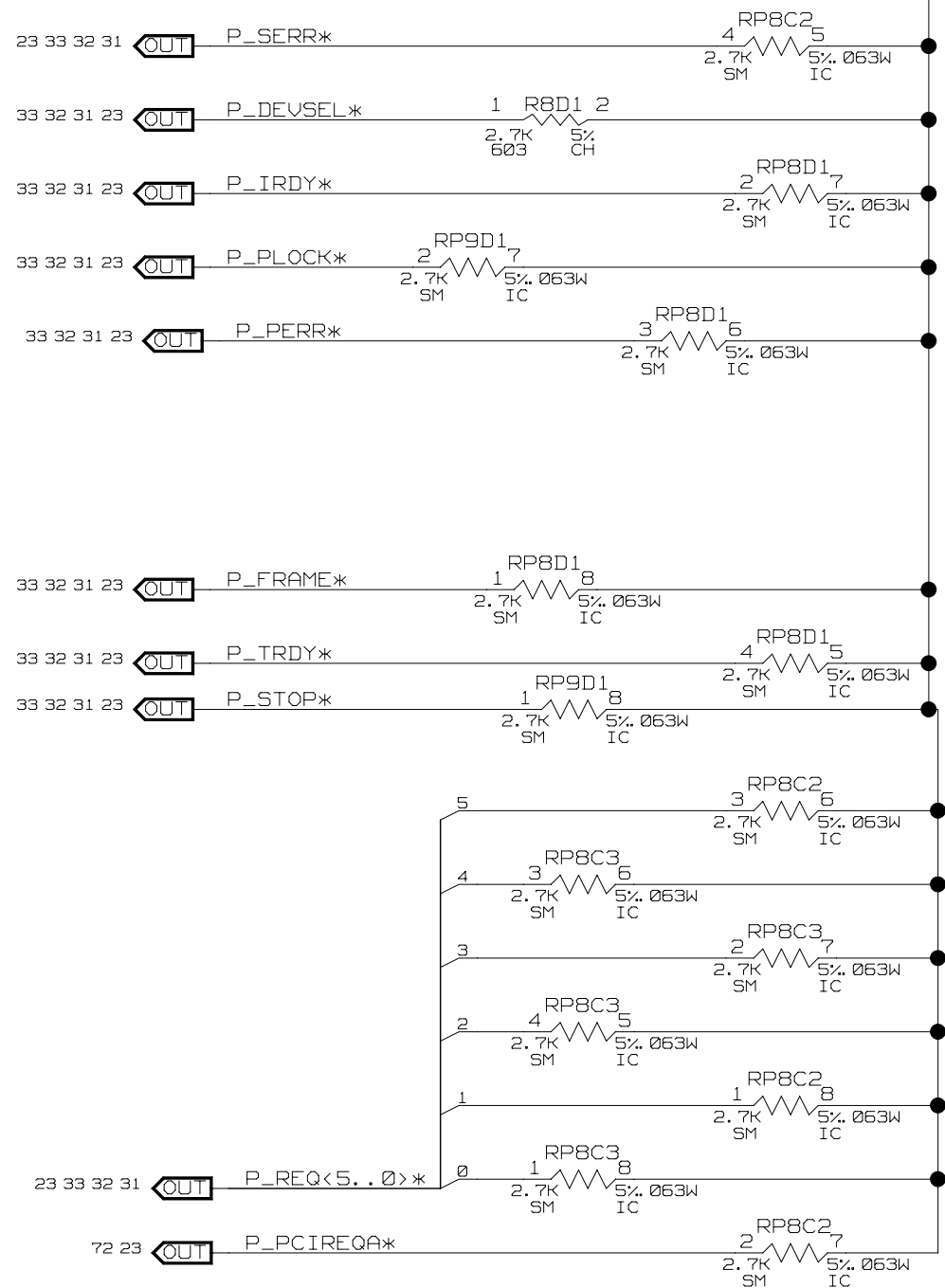
PCI SLOT DECOUPLING



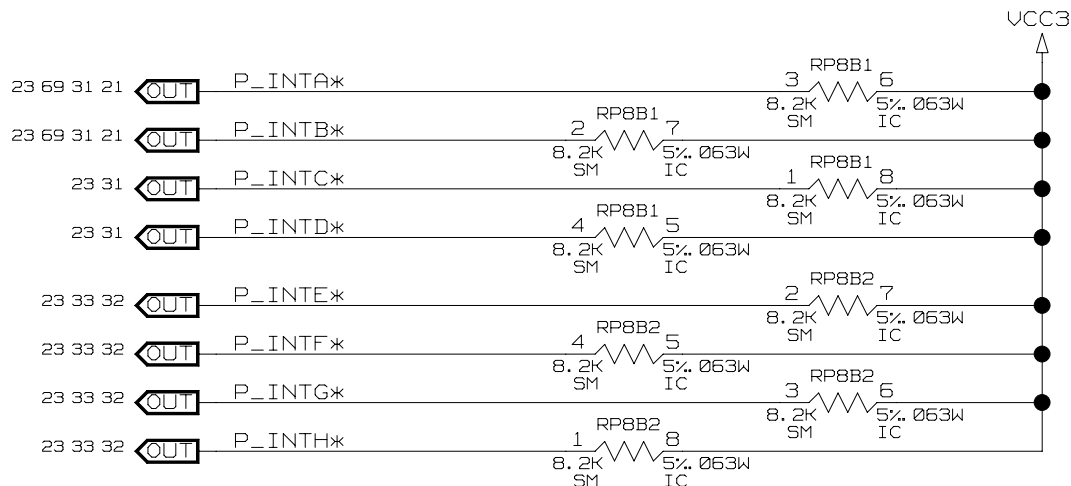
NOTE
PLOCK, PSTOP, PTRDY, PIRDY,
PFRAME, PPERR MAY NEED
TO BE CHANGED TO A 3.3V PU

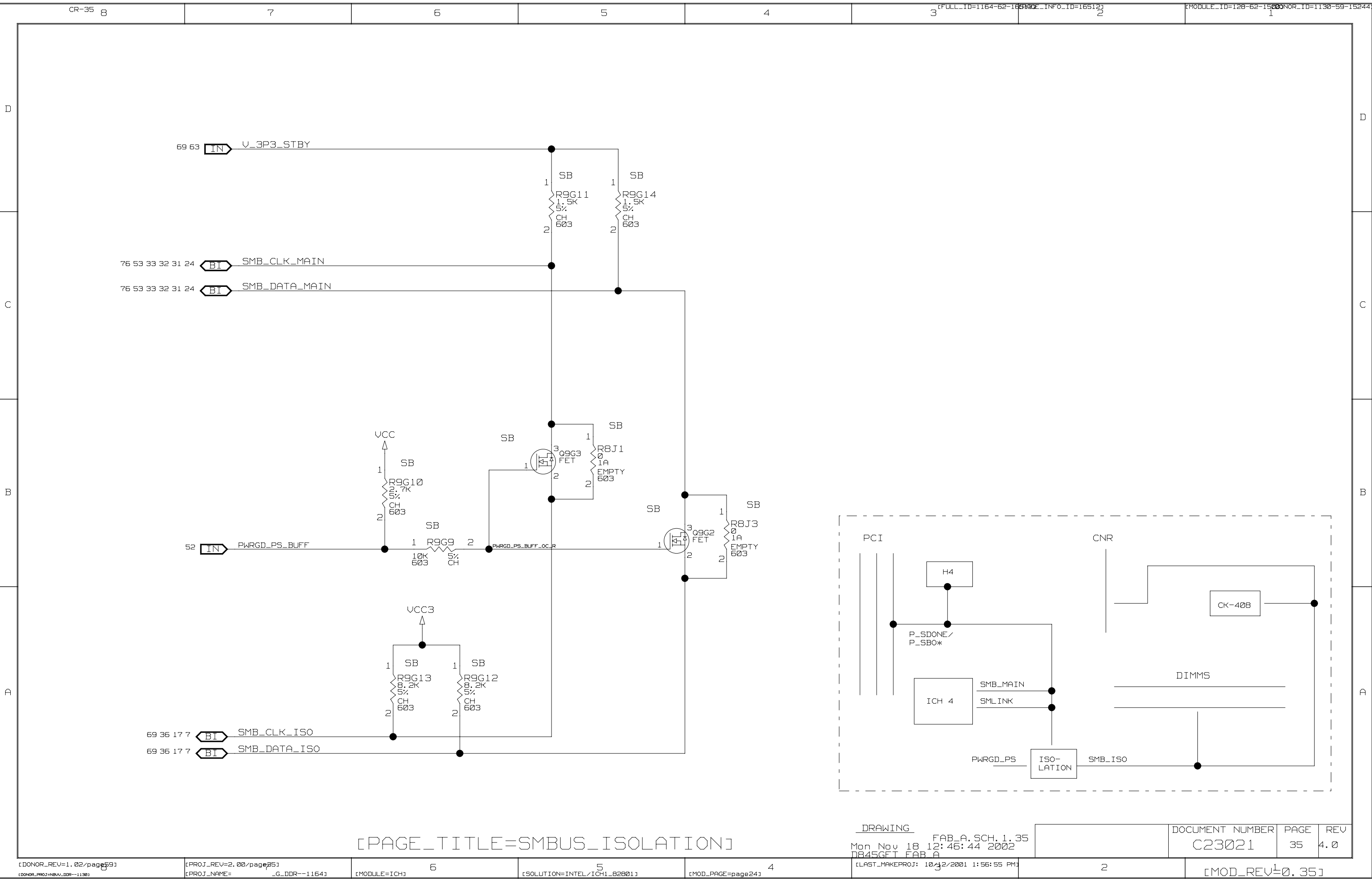


PCI PULL-UPS



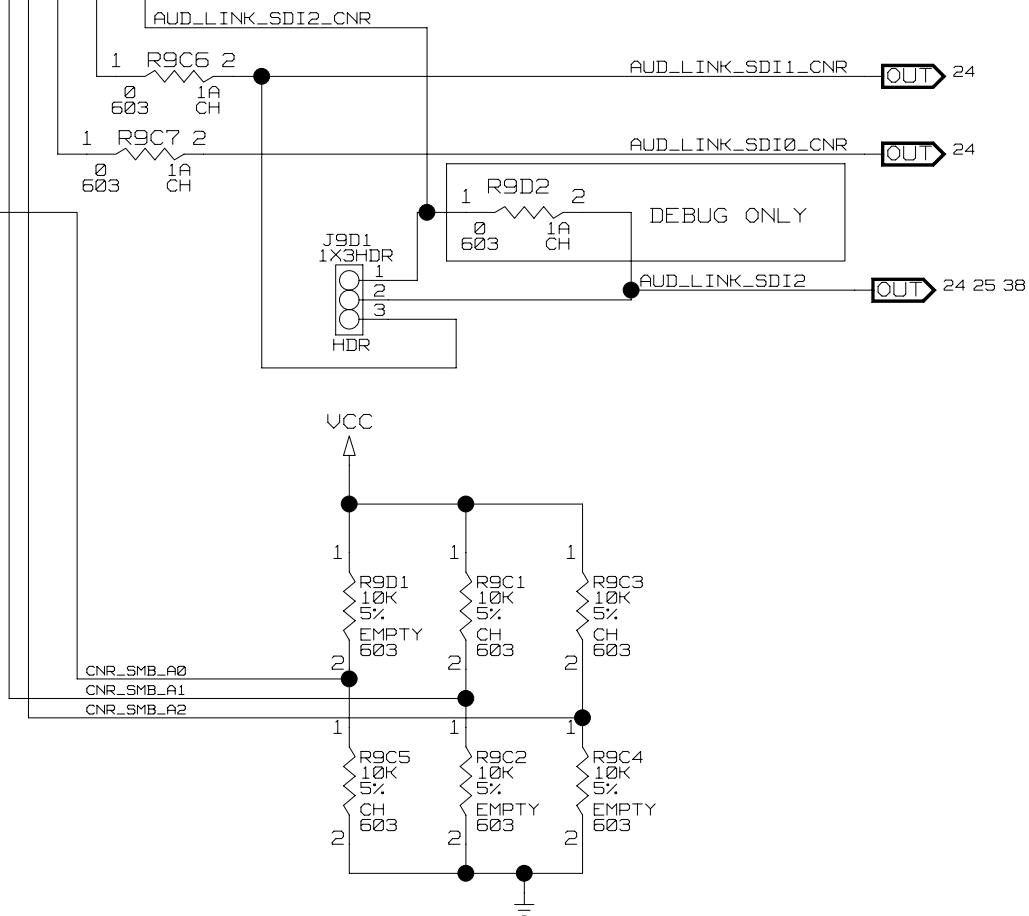
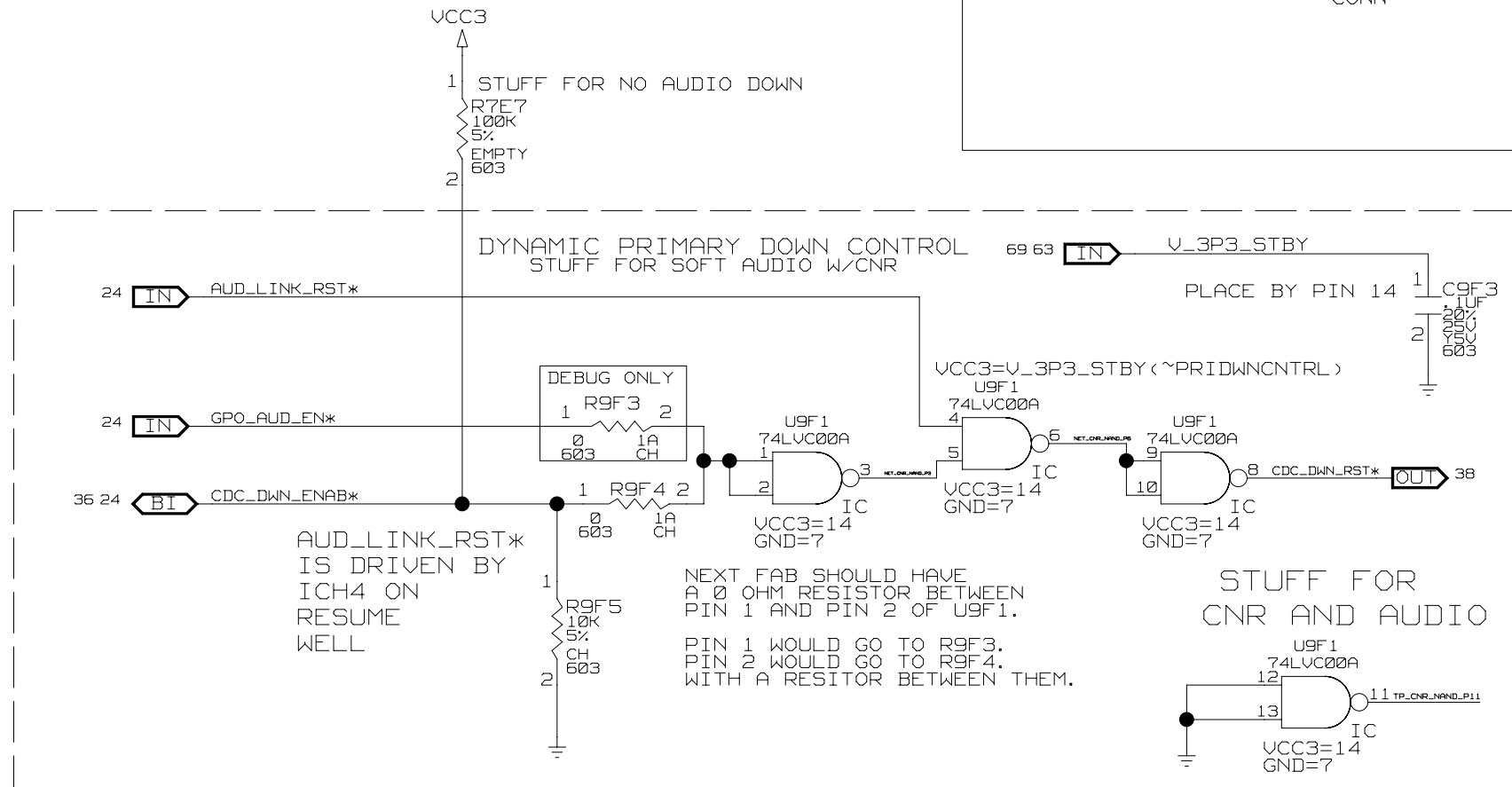
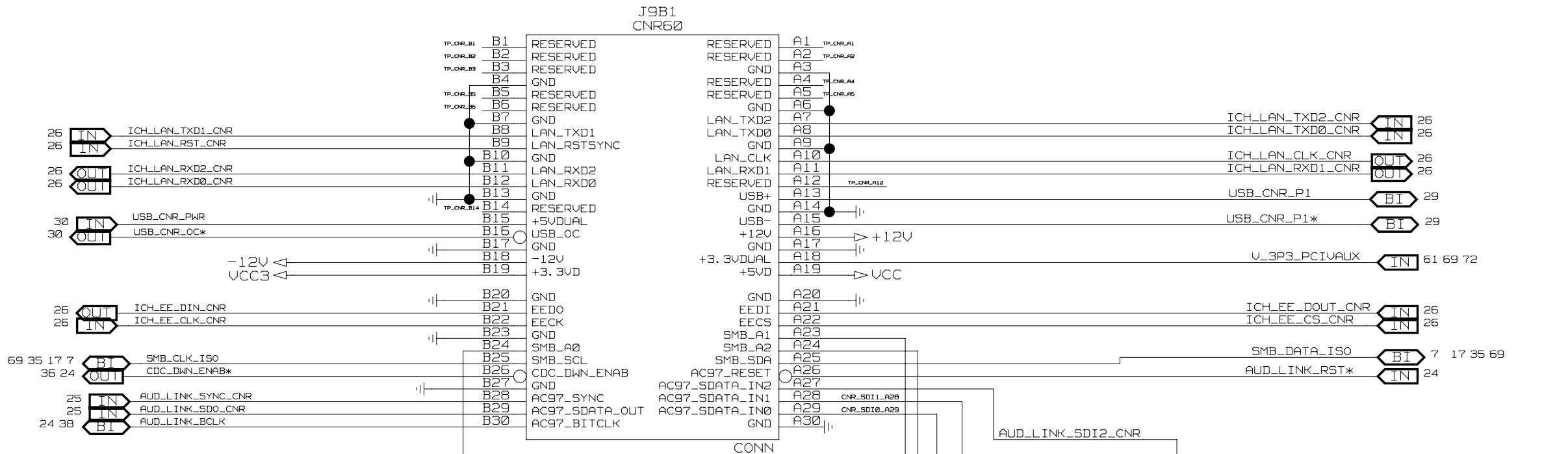
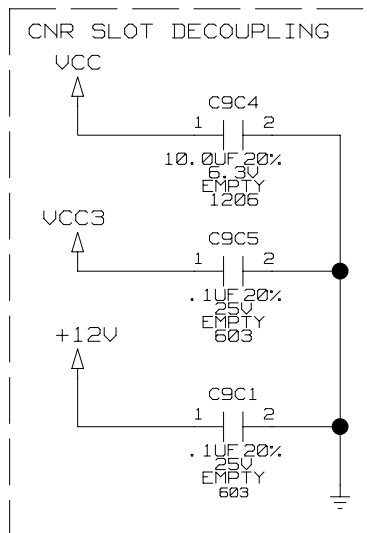
SPARE SECTIONS





NOTE: CNR SPEC SAYS SMBUS CONTROLLER NOT POWERED BY 3V STBY

SMB ADDRESS: 1101110
WRITE DC
READ DD



[MODULE=AUDIO]

D

C

B

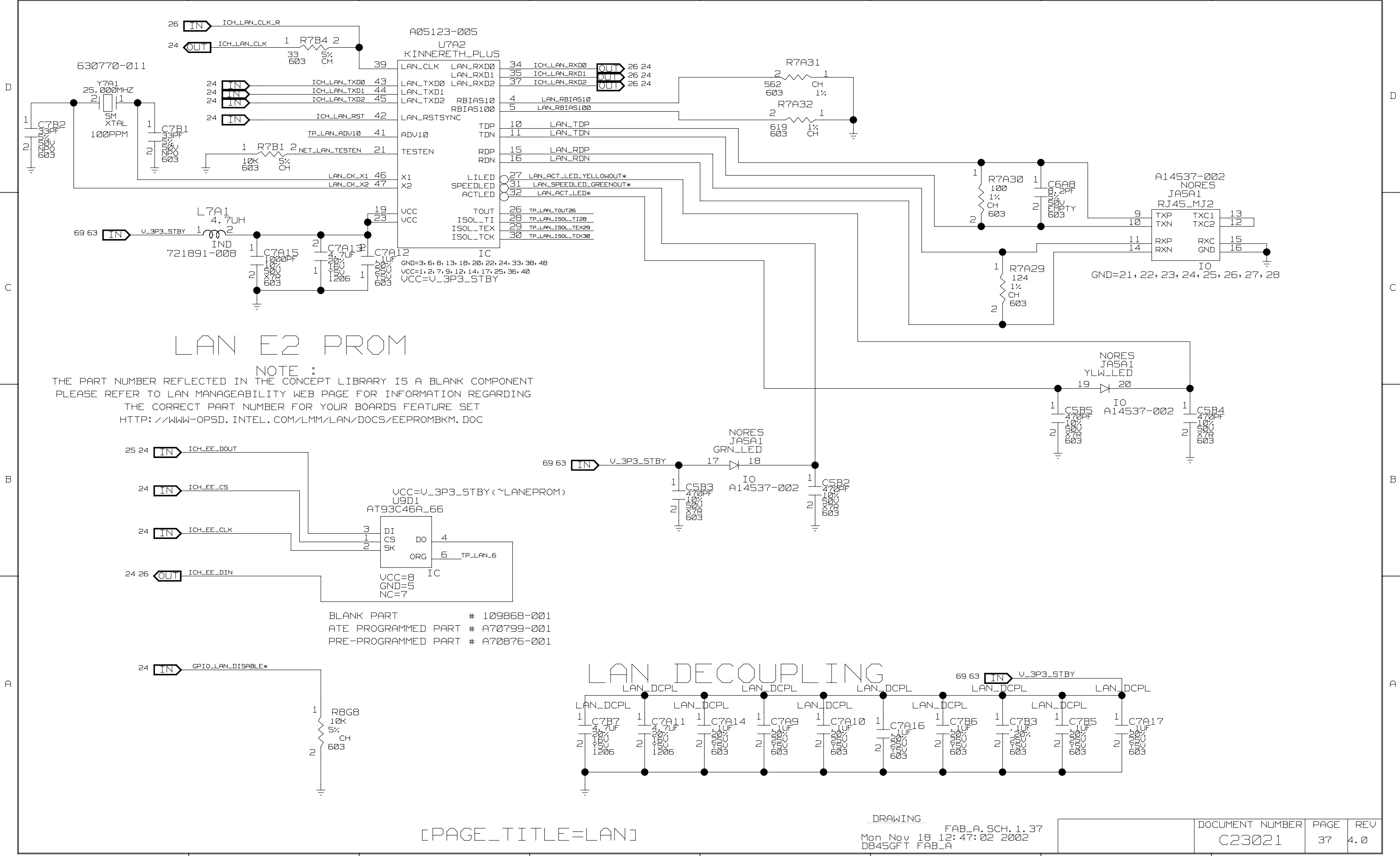
A

D

C

B

A



[PAGE_TITLE=LAN]

DRAWING

FAB_A.SCH.1.37
Mon Nov 18 12:47:02 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	37	4.0

D

C

B

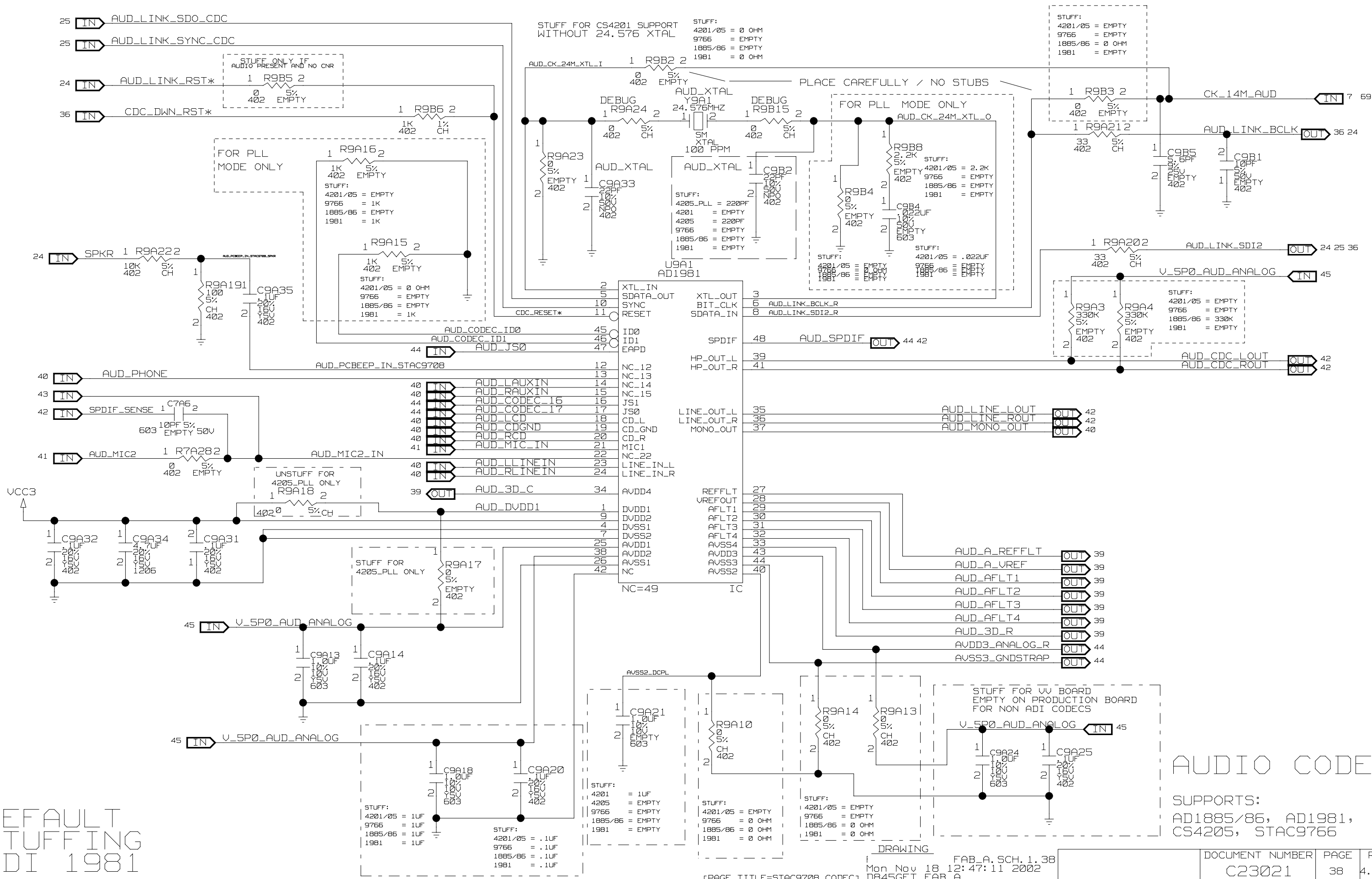
A

D

C

B

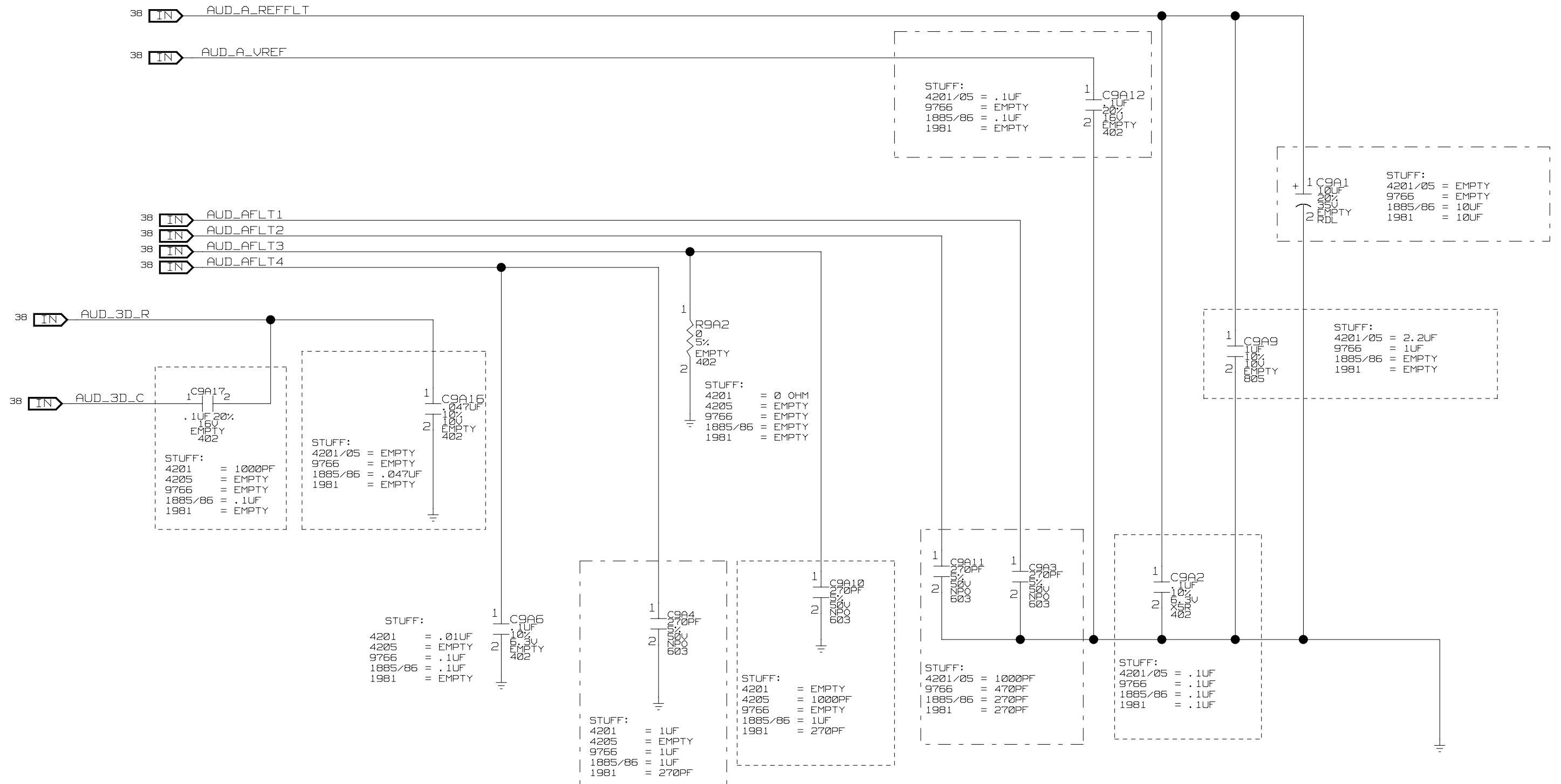
A



DEFAULT
STUFFING
ADI 1981

AUDIO CODEC
SUPPORTS:
AD1885/86, AD1981,
CS4205, STAC9766

KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC.



```
CODEC FILTER CAPS:
1981, 1885/86, 4205, 9766
AUDIO SUBMODULE 2
```

```

DEFAULT
STUFFING
ADI 1981

```

[MODULE=AUDIO]

[SOLUTION=AUDIO/AUDIO]

[MOD_PAGE=PAGE41]

[MOD_REV=REV0_60C]

[PAGE_TITLE=CODEC]
[LAST_MAKEGOLD: 6/14/99 9:20:55am]

DRAWING

FAB_A.SCH.1.39

Mon Nov 18 12:47:20 2002
D845GFT FAB A

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[LAST_MAKEPROJ: 10/12/2001 1:56:58 PM]

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DOCUMENT NUMBER	1
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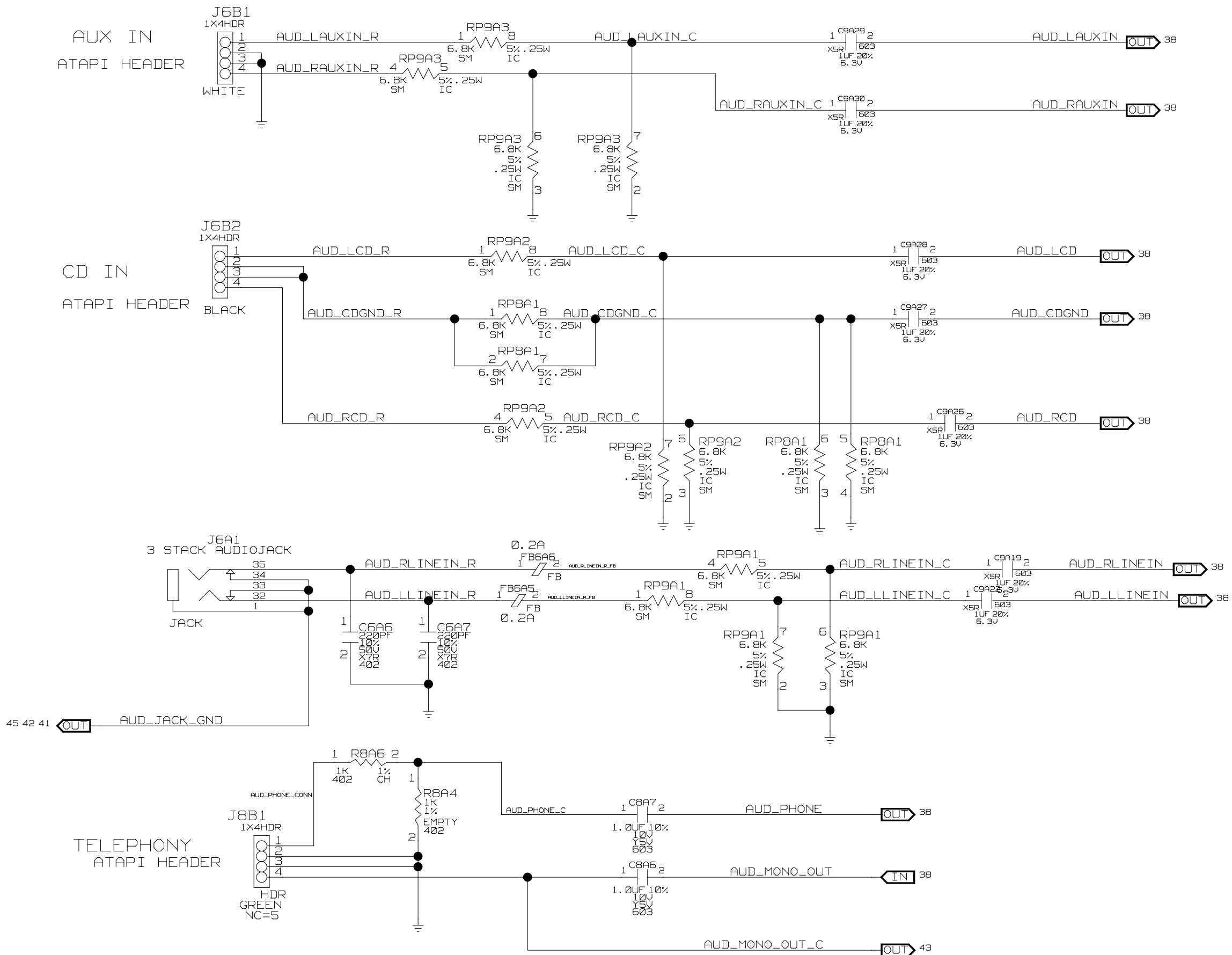
C23021

PAGE |

39 4

REV

☐



AUDIO SUBMODULE 5

DRAWING

FAB_A.SCH.1.40

Mon Nov 18 13:50:34 2002

D845GFT FAB_A

[LAST_MAKEPROJ: 10/32/2001 1:56:58 PM]

DOCUMENT NUMBER

C23021

PAGE

40

REV

4.0

[MODULE=AUDIO]

[SOLUTION=AUDIO/AUDIO]

[MOD_PAGE=PAGE27]

[MOD_REV=REV0_60C]

[PAGE_TITLE=ATX_ATAPI_CONNECTORS]

[LAST_MAKEGOLD: 6/14/99 9:19:23am]

[DONOR_REV=1.02/page411]

[DONOR_PROJ=NBVV_DDR--1130]

[PROJ_REV=2.00/page410]

[PROJ_NAME=_G_DDR--1164]

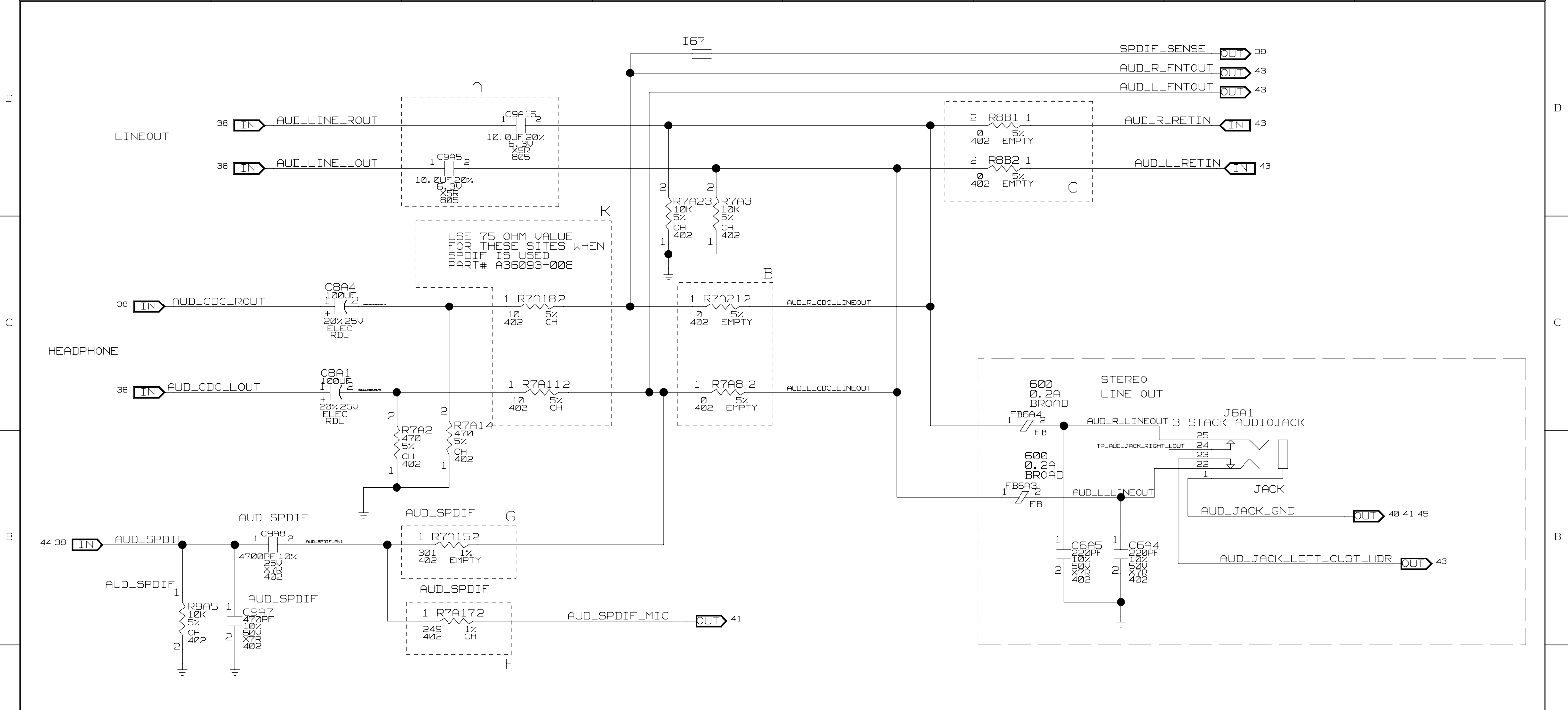
6

5

4

2

1

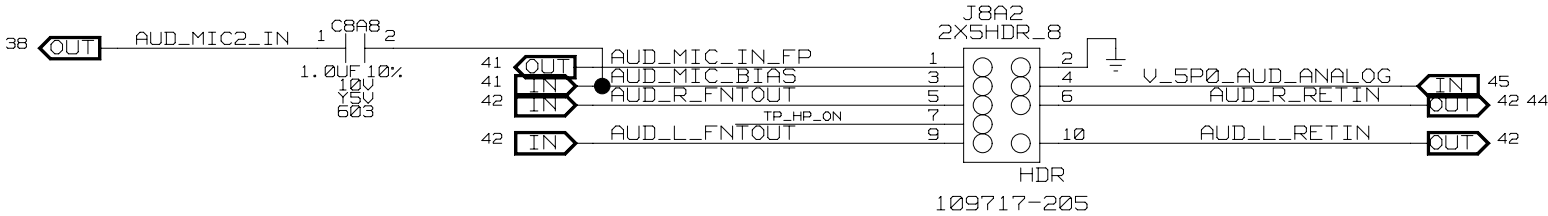


	BP ONLY	FP-->BP	SPDIF	BP LO	BP MIC
HEADPHONE	STUFF B	STUFF C	F	EMPTY	STUFF
	EMPTY A, C	EMPTY A, B	G	STUFF	EMPTY
			H	EMPTY	110 OHM
LINEOUT	STUFF A	N/A	J	STUFF	EMPTY
	EMPTY B, C		K	75 OHM	10 OHM

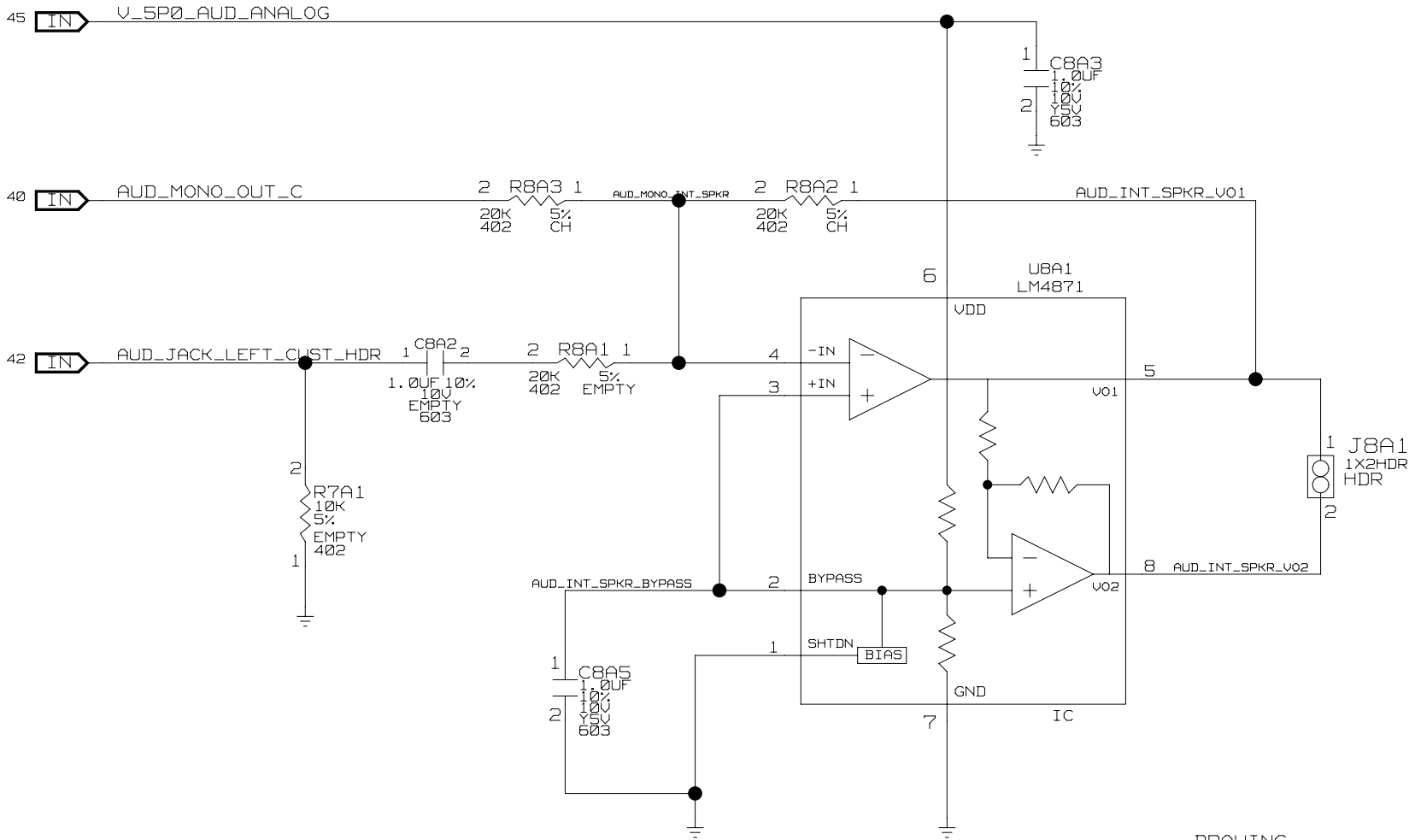
NOTE:
ADD EMI CAPS

NOTE:
FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION

AUDIO FRONT PANEL
PLACE NEAR AUDIO CIRCUIT



INTERNAL SPEAKER CIRCUIT



[PAGE_TITLE=AUIDO_FP]

DRAWING
FAB_A.SCH.1.43
Mon Nov 18 12:29:03 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	43	4.0

MIC JACK SENSE

NOTE:
FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION

GPIO LOCATIONS:

NOT CONNECTED

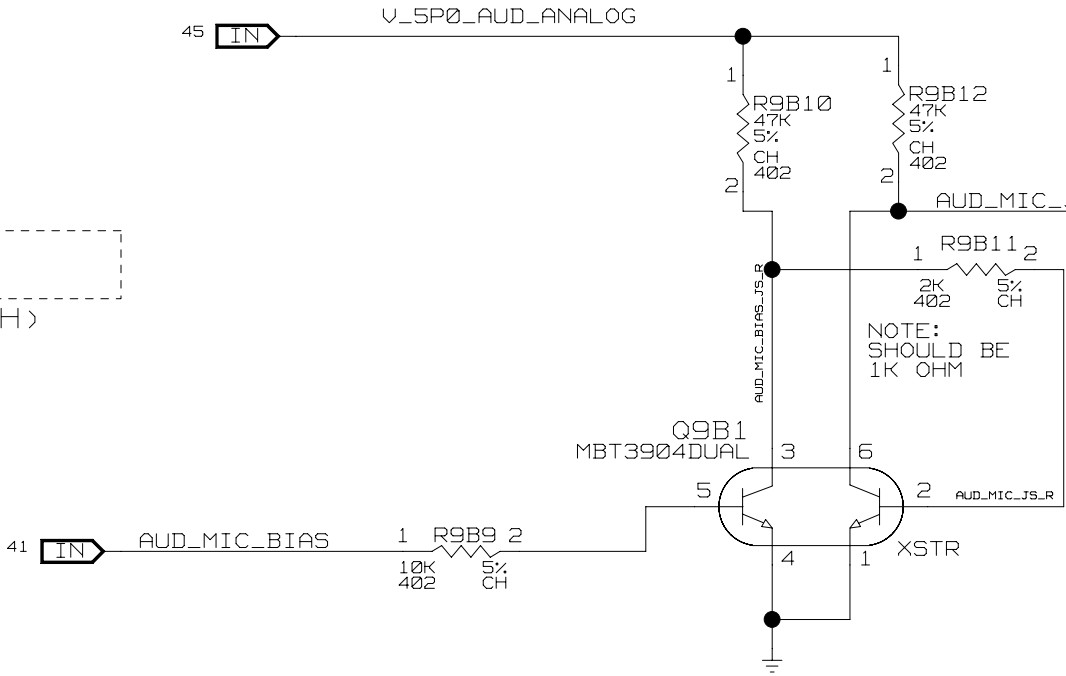
4205: 43, 44, 41, 40, 39

1981: 16, 17 (ACTIVE HIGH)

9766: 43, 44

4291: NONE

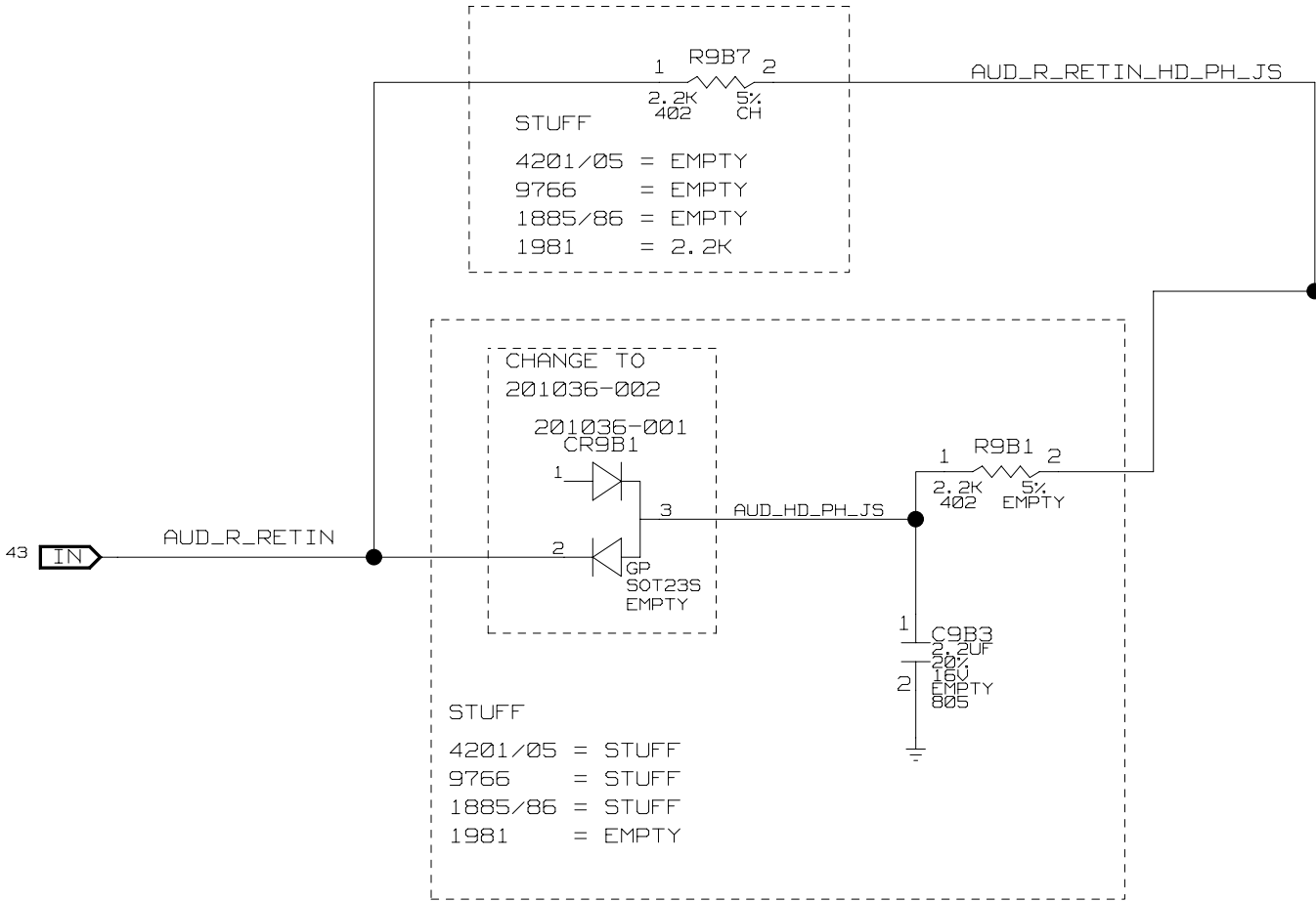
1885/86: 47, 48



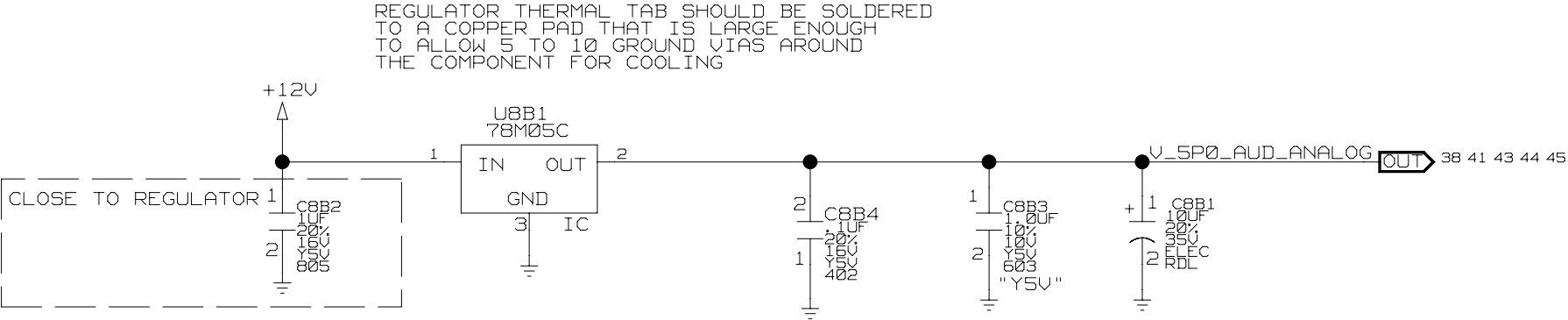
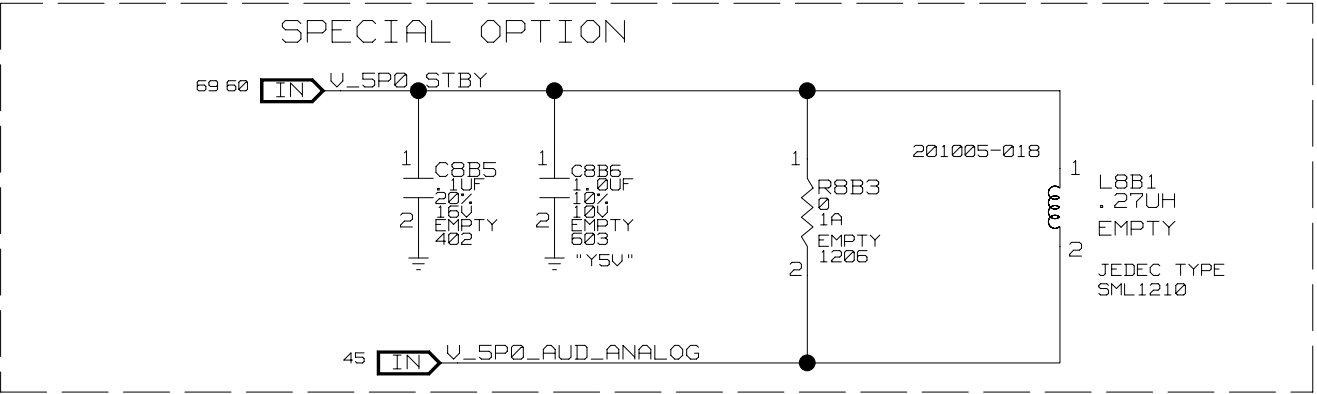
NOTE:
TOP RESISTOR STUFF: 1981
MIDDLE RESISTOR STUFF: 9766/4205
BOTTOM RESISTOR STUFF: 1885/86

HEADPHONE JACK SENSE

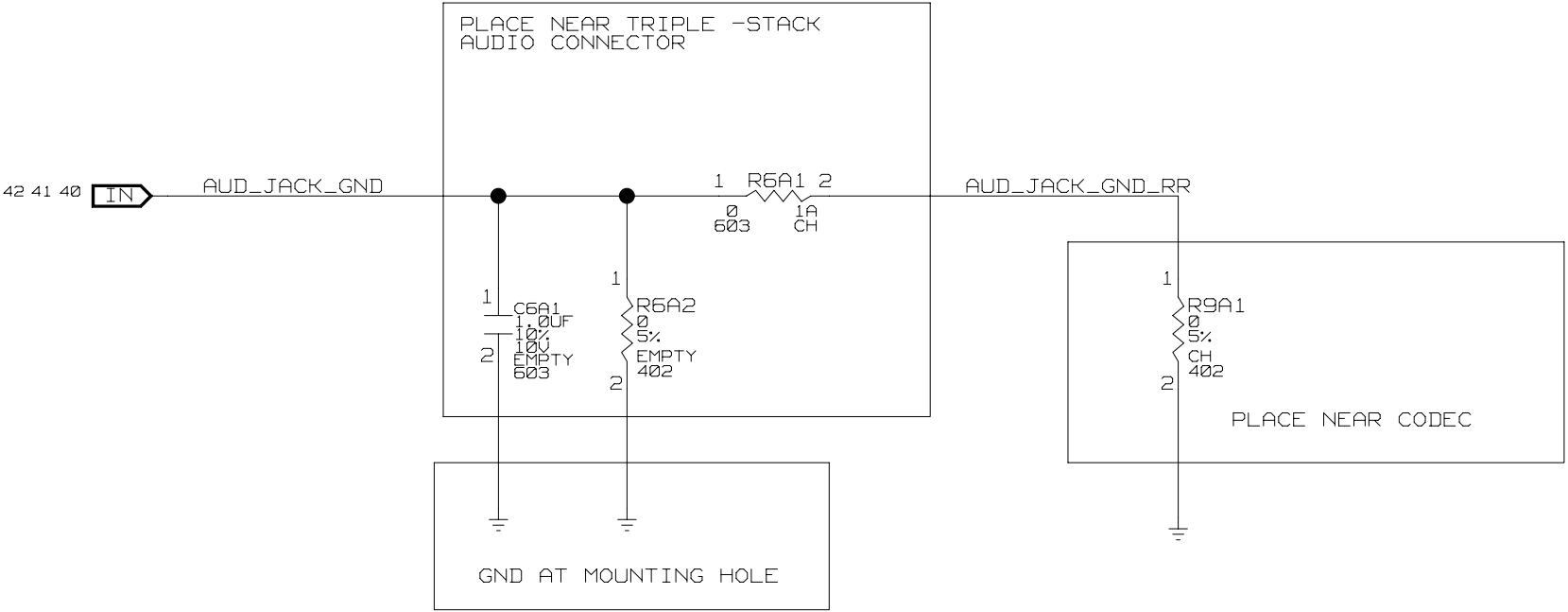
NOTE:
TOP RESISTOR STUFF: 1981
MIDDLE RESISTOR STUFF: 9766/4205
BOTTOM RESISTOR STUFF: 1885/86



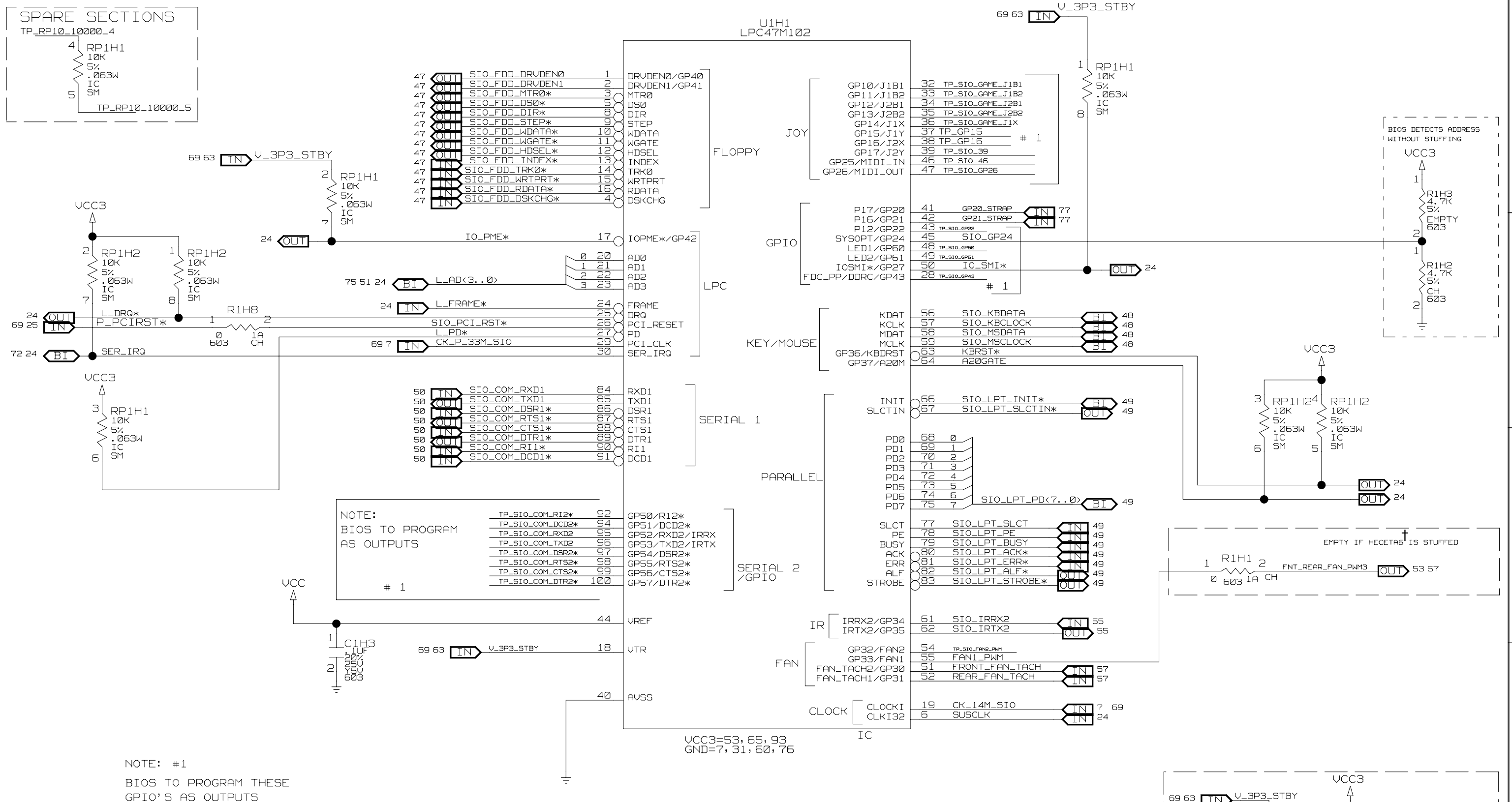
DEFAULT
STUFFING
ADI 1981



NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO CAPS AND THEN THROUGH SEVERAL VIAS TO V_5P0_AUD_ANALOG



[PAGE_TITLE=AUDIO_VREG]

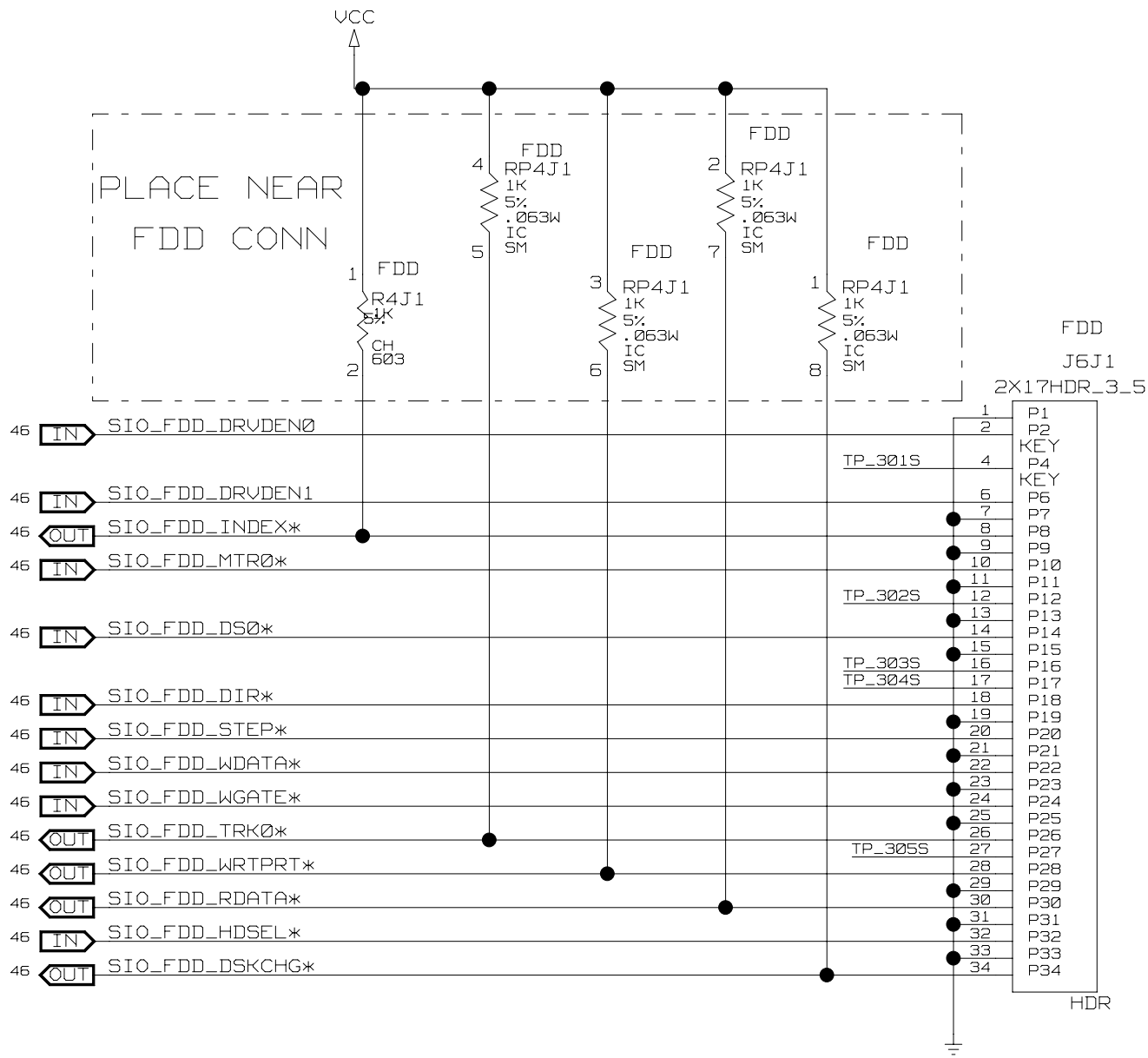


DRAWING

FAB_A.SCH.1.46
Mon Nov 18 13:50:51 2002
D845GFT FAB_A

PLACE NEAR SMC DEVICE PINS 56, 65, 93, 125

DOCUMENT NUMBER	PAGE	REV
C23021	46	4.0



DRAWING

FAB_A.SCH.1.47
Mon Nov 18 13:51:00 2002
D845GFT FAB_A

DOCUMENT NUMBER
C23021

PAGE
47

REV
4.0

D

D

C

C

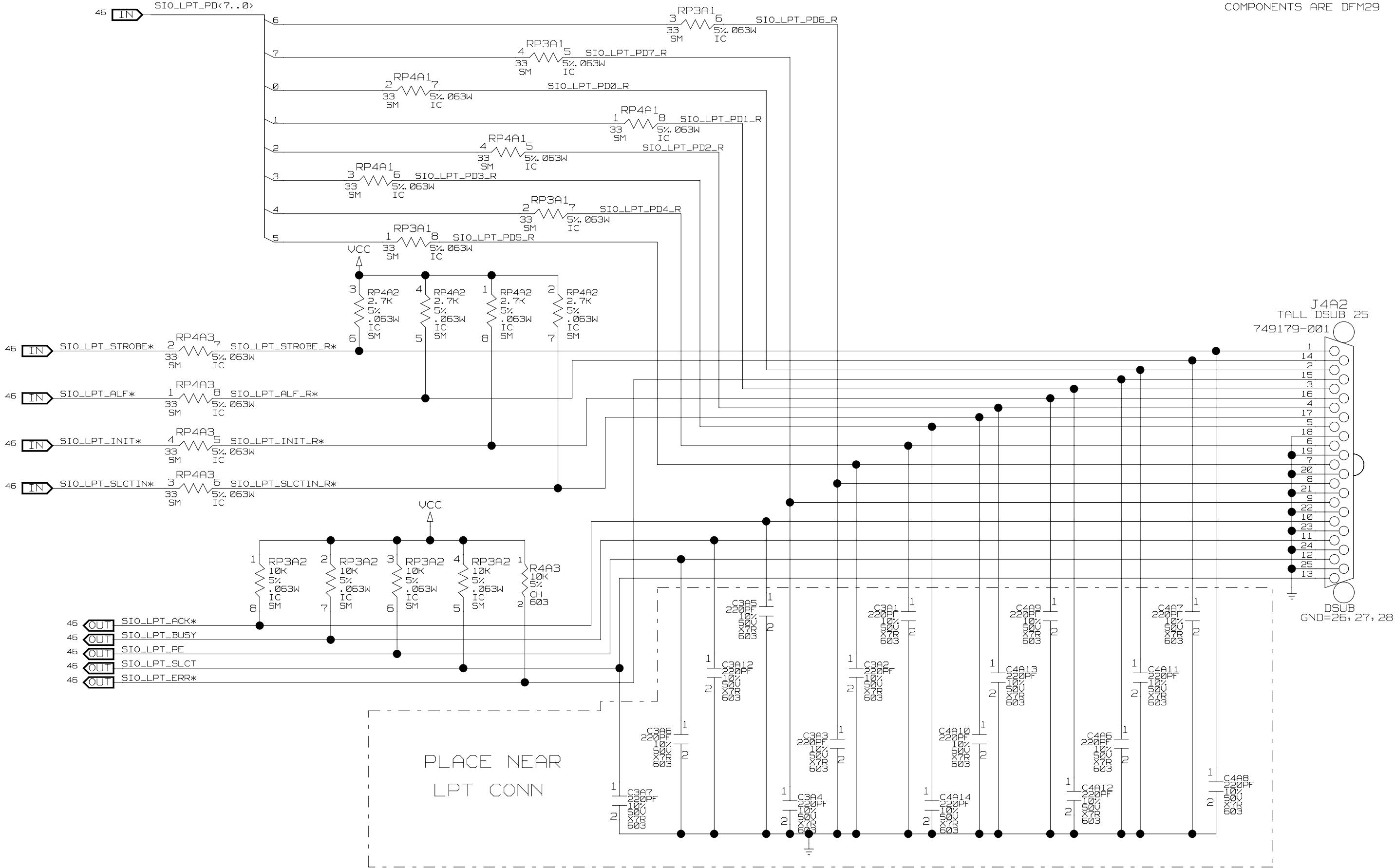
B

B

A

A

COMPONENTS ARE DFM29



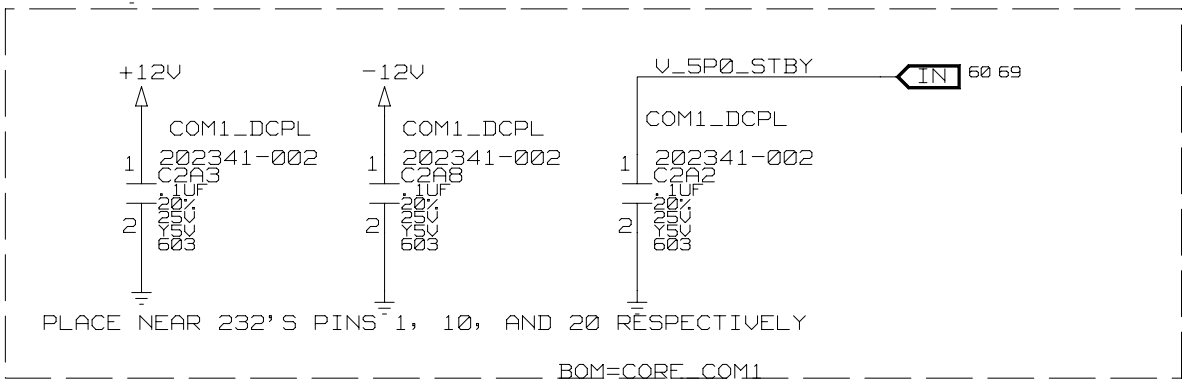
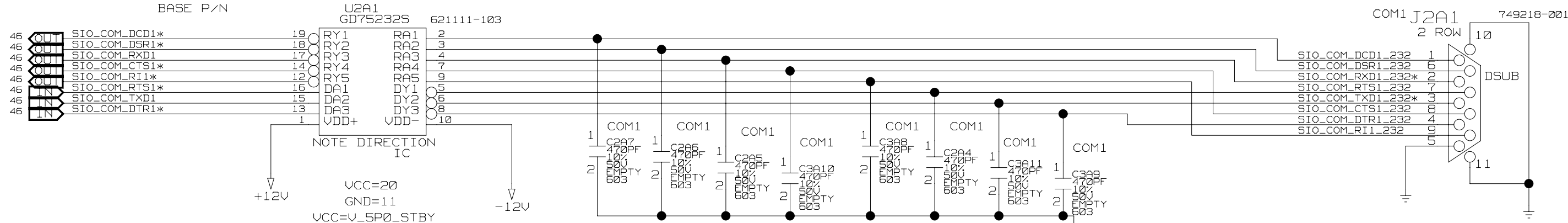
DRAWING

FAB_A.SCH.1.49
Mon Nov 18 12:29:58 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	49	4.0

COMPONENTS ARE DFM29

SERIAL PORT A



DRAWING

FAB_A. SCH. 1. 50

Mon Nov 18 12:30:07 2002
D845GFT FAB_A

DOCUMENT	NUMBER	PAGE	REV
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C23021

PAGE	REV
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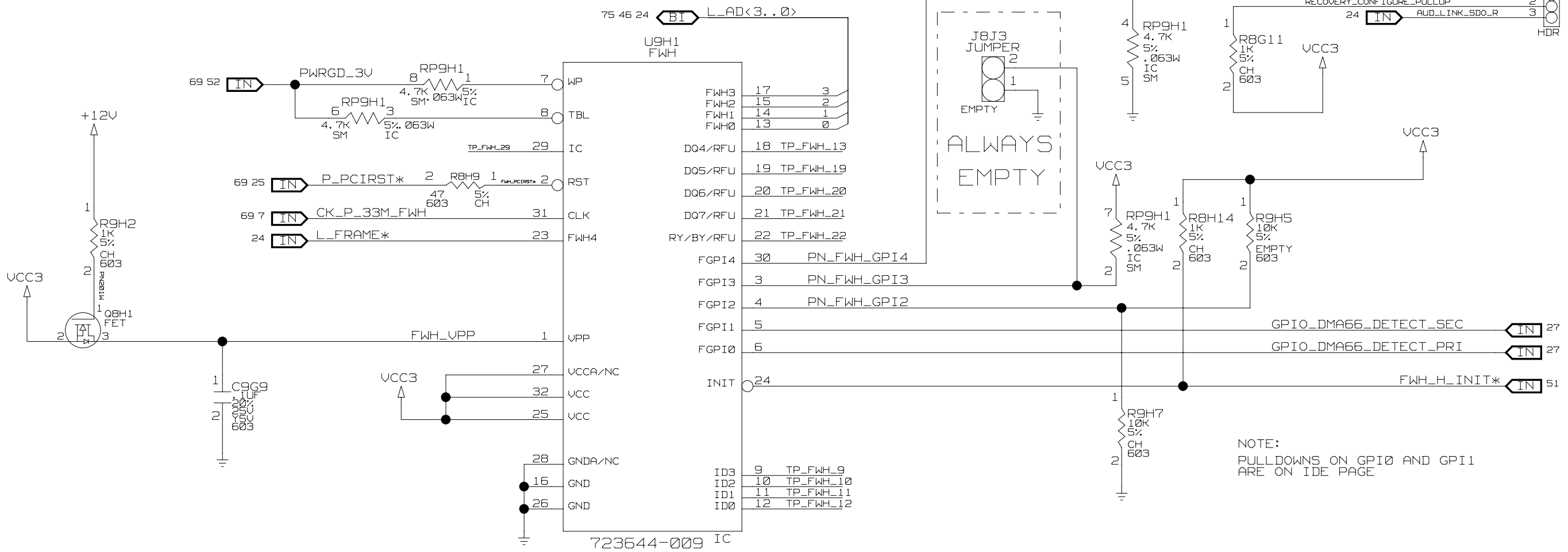
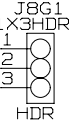
C

B

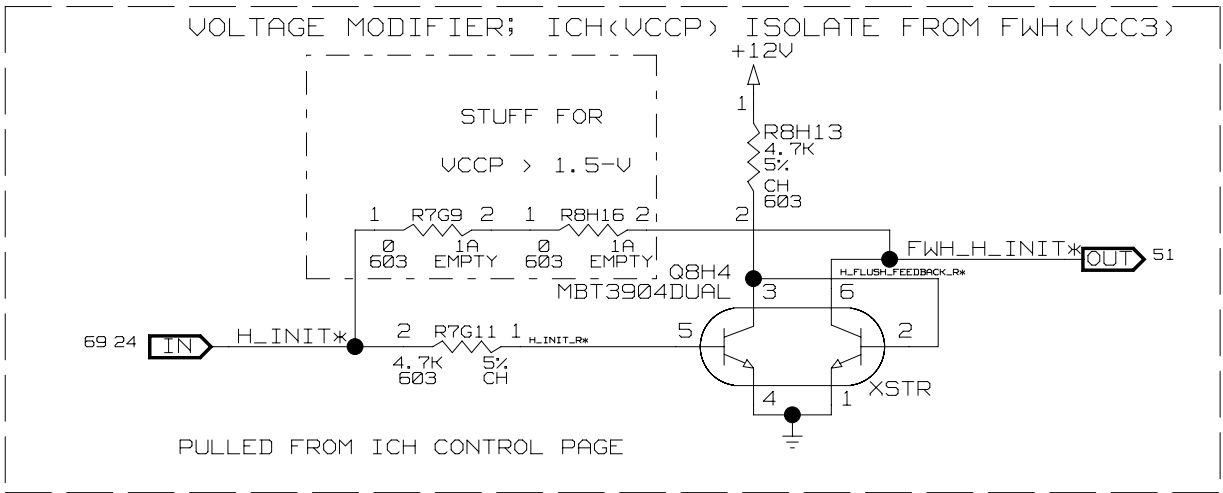
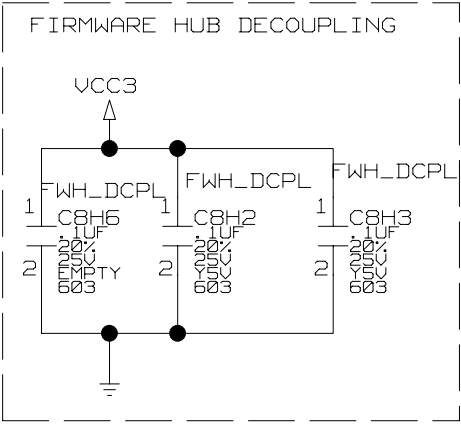
A

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE



NOTE:
PULLDOWNS ON GPIO AND GPI1
ARE ON IDE PAGE



FIRMWARE HUB

DRAWING

FAB_A.SCH.1.51

Mon Nov 18 13:51:18 2002

D845GFT FAB_A

LAST MAKEGOLD: 9/10/99 1:12:46pm

LAST_MAKEPROJ: 10/3/2001 1:57:03 PM

DOCUMENT NUMBER	PAGE	REV
C23021	51	4.0

GLUECHIP4

GLUE4 INPUTS

PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	VCCP REF
6	GP1_INA	VCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	5IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	5IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HD*	5IU
26	SCSI*	5IU
27	SECONDARY_HD*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
53	VCCP_VREF	AI
54	STRAP	3IU
55	GP3_IN	5I

D

C

B

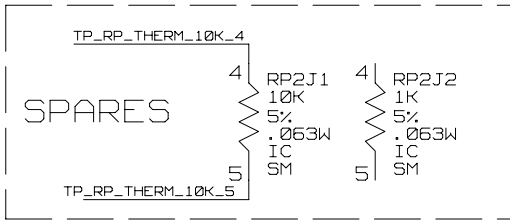
A

D

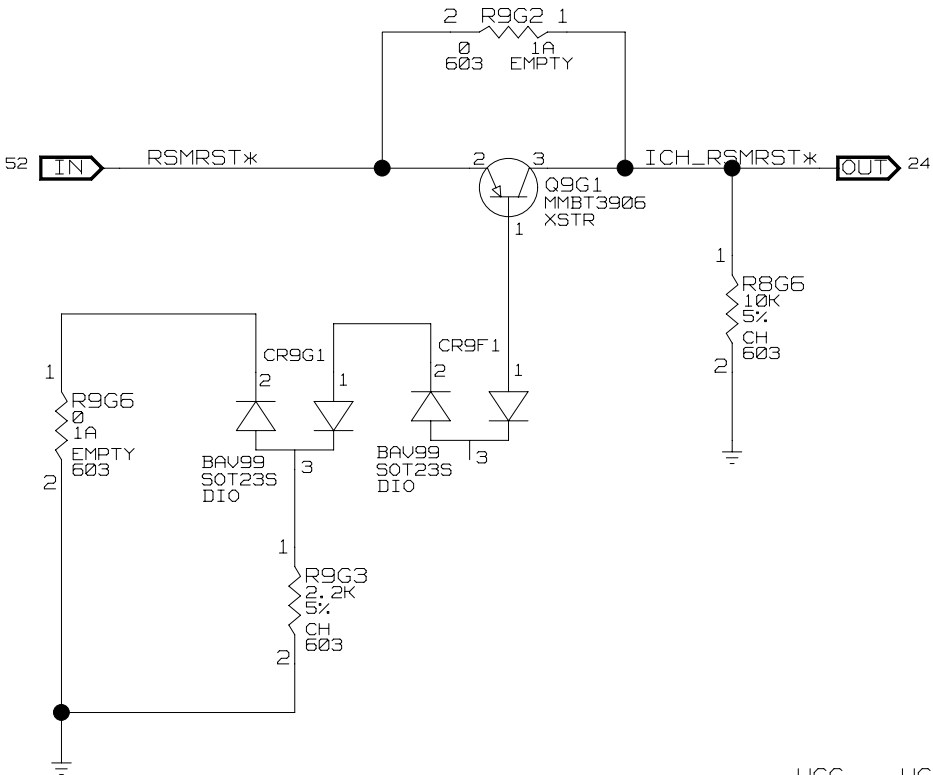
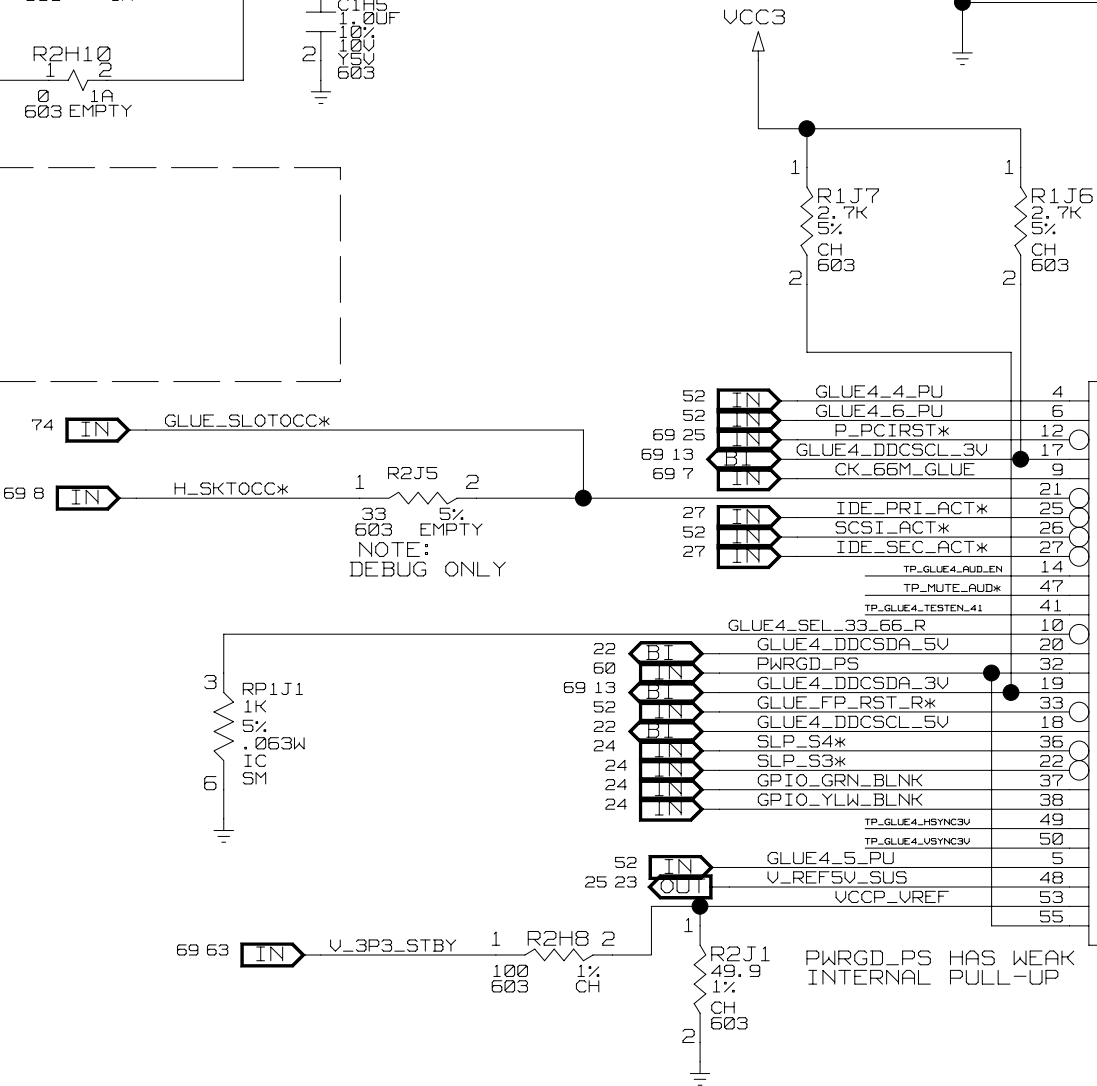
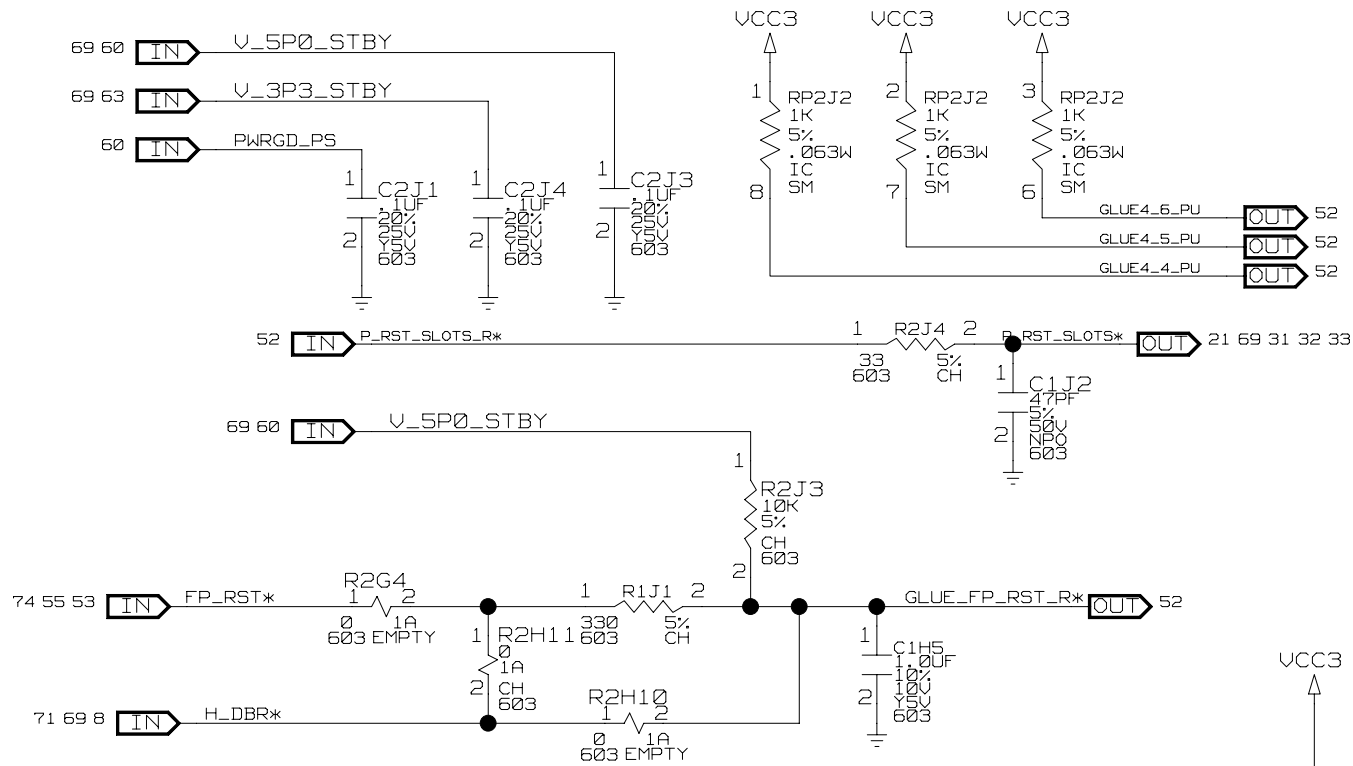
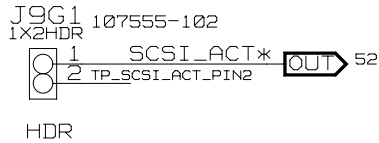
C

B

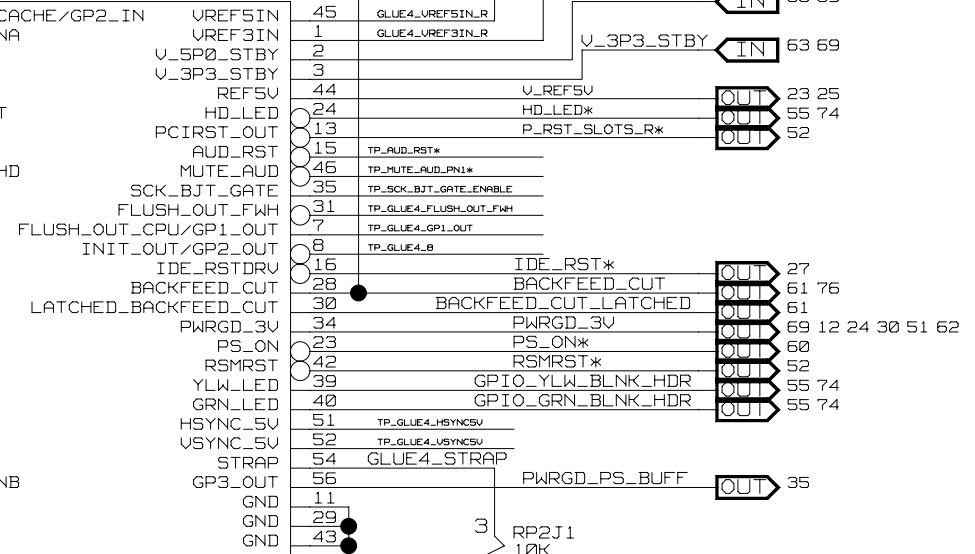
A



SCSI ACTIVITY LED



U2J1 GLUECHIP4 A12878-002



[PAGE_TITLE=GLUE4]

DRAWING

FAB_A, SCH. 1.52
Mon Nov 18 12:30:26 2002
DB45GFT FAB A

DOCUMENT NUMBER
C23021

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52

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4.0

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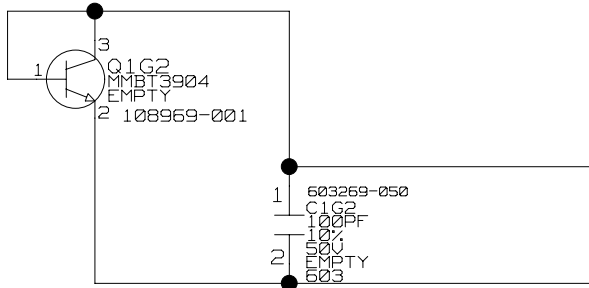
C

B

A

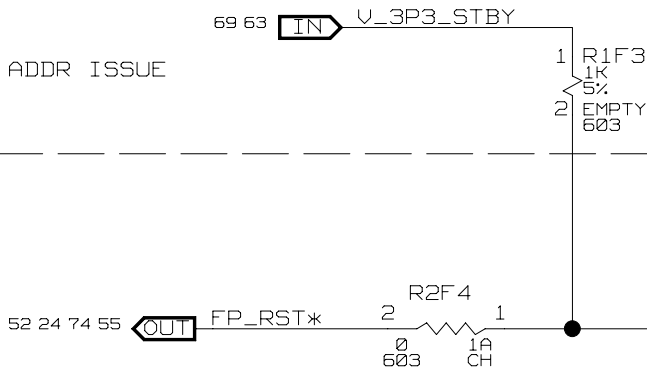
CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS

CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP

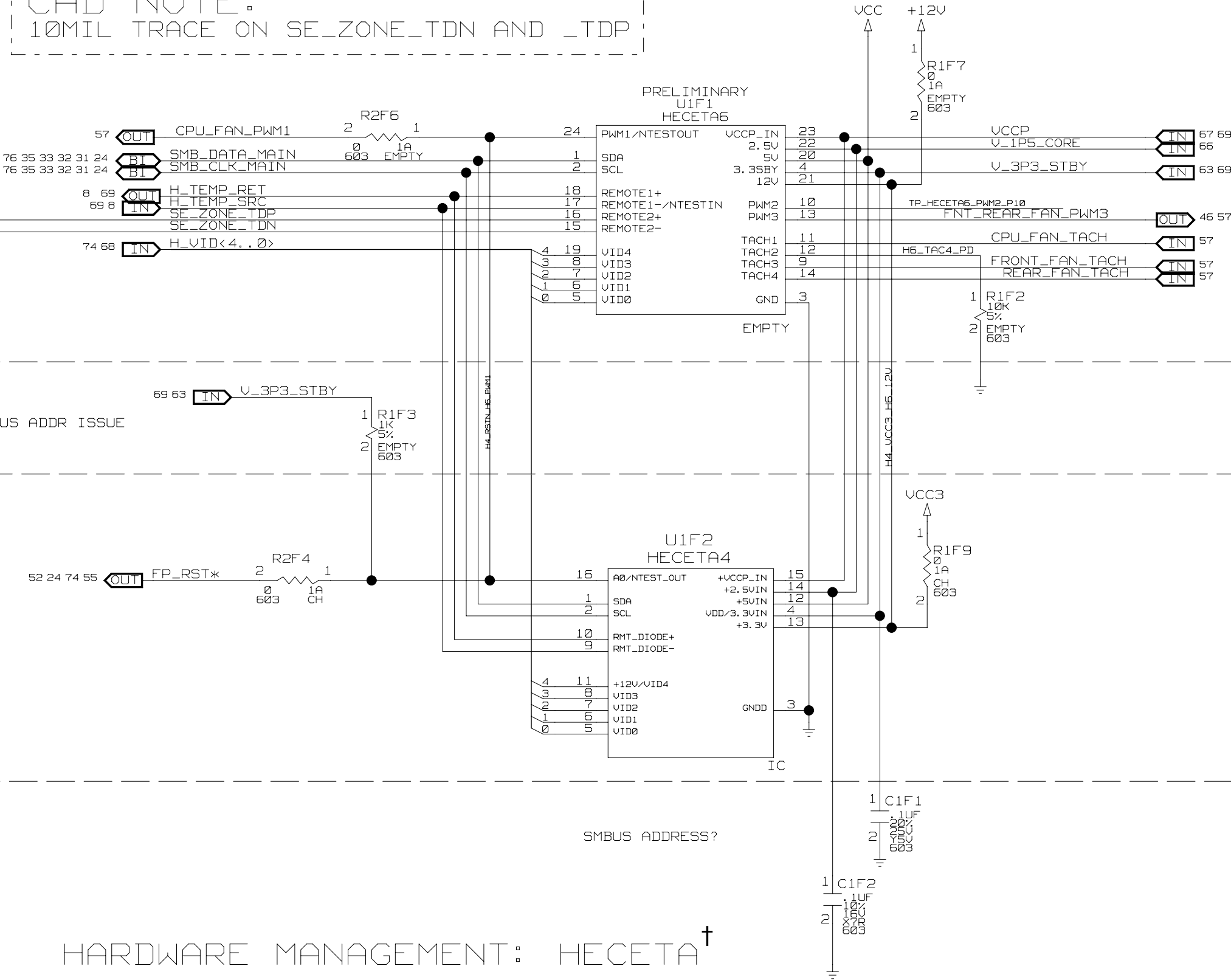


ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4

NOTE
FOR PHILLIPS H4 SMBUS ADDR ISSUE



ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6



SMBUS ADDRESS?

HARDWARE MANAGEMENT: HECETA†

DRAWING

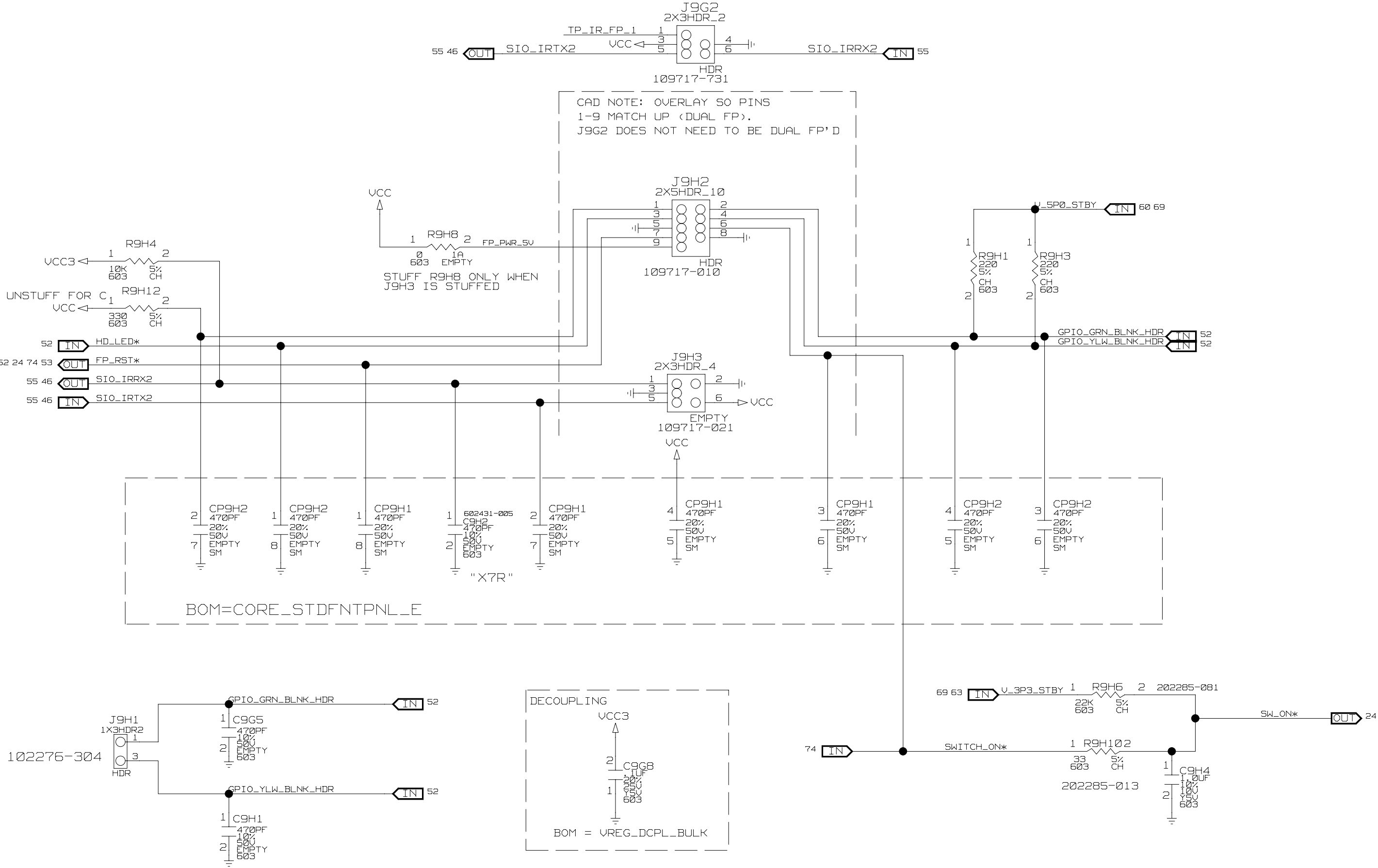
FAB_A.SCH.1.53

Mon Nov 18 13:51:27 2002
D845GFT FAB_A

[PAGE_TITLE=HECETA]

ROOM=HWM_HECETA4
BOM=HWM_HECETA4

DOCUMENT NUMBER	PAGE	REV
C23021	53	4.0

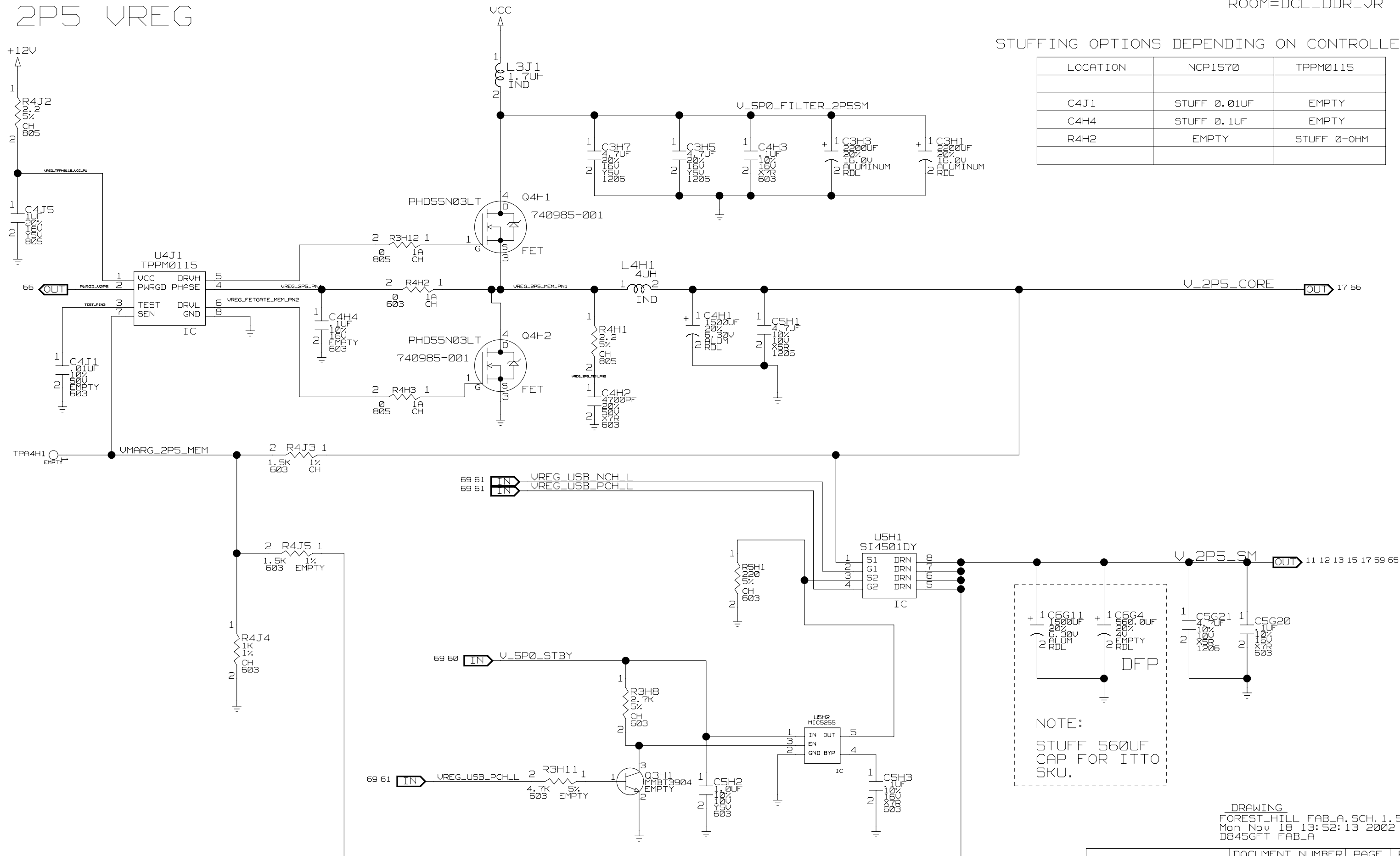


[PAGE_TITLE=STD_FRONT_PANEL_HDR]

ROOM=DCL_DDR_VR

STUFFING OPTIONS DEPENDING ON CONTROLLER

LOCATION	NCP1570	TPPM0115
C4J1	STUFF 0.01UF	EMPTY
C4H4	STUFF 0.1UF	EMPTY
R4H2	EMPTY	STUFF 0-OHM

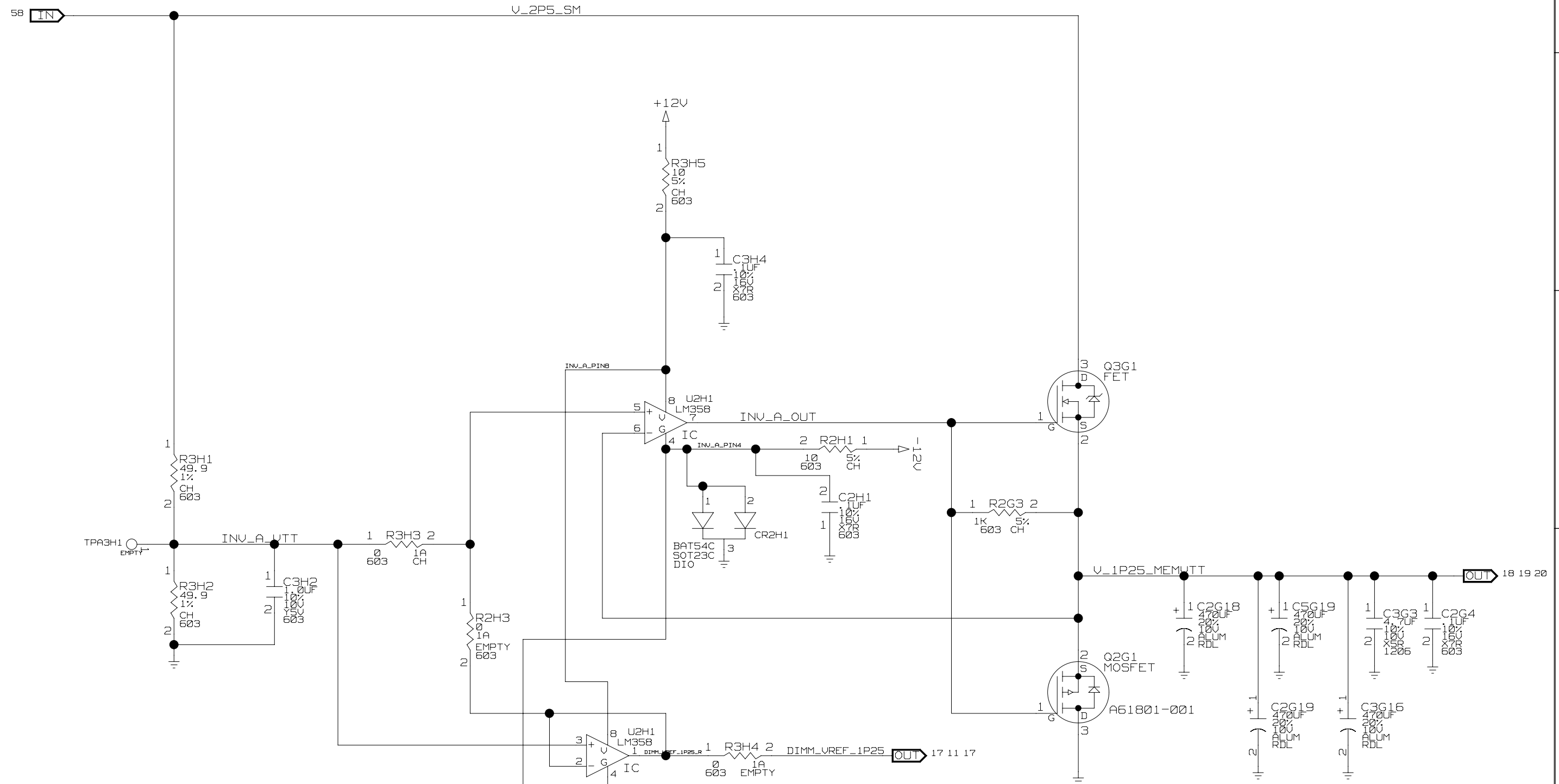


DRAWING
FOREST_HILL FAB_A.SCH.1.58
Mon Nov 18 13:52:13 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	58	4.0

1. 25V DDR

ROOM=DCL_DDR_VR

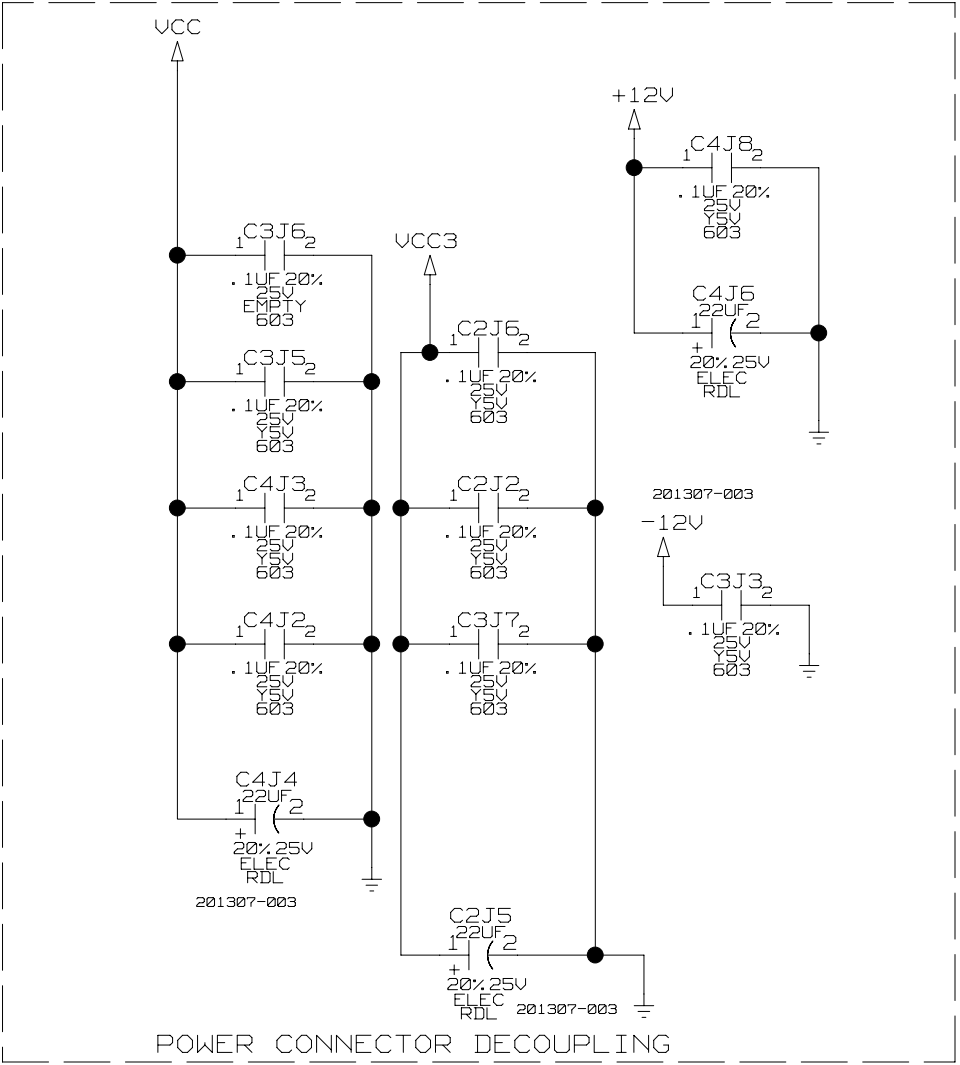
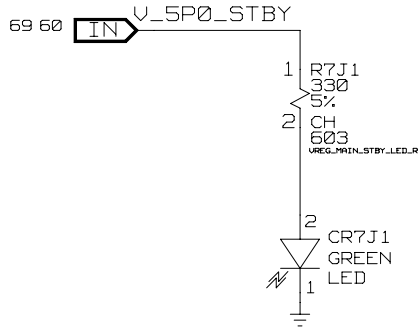
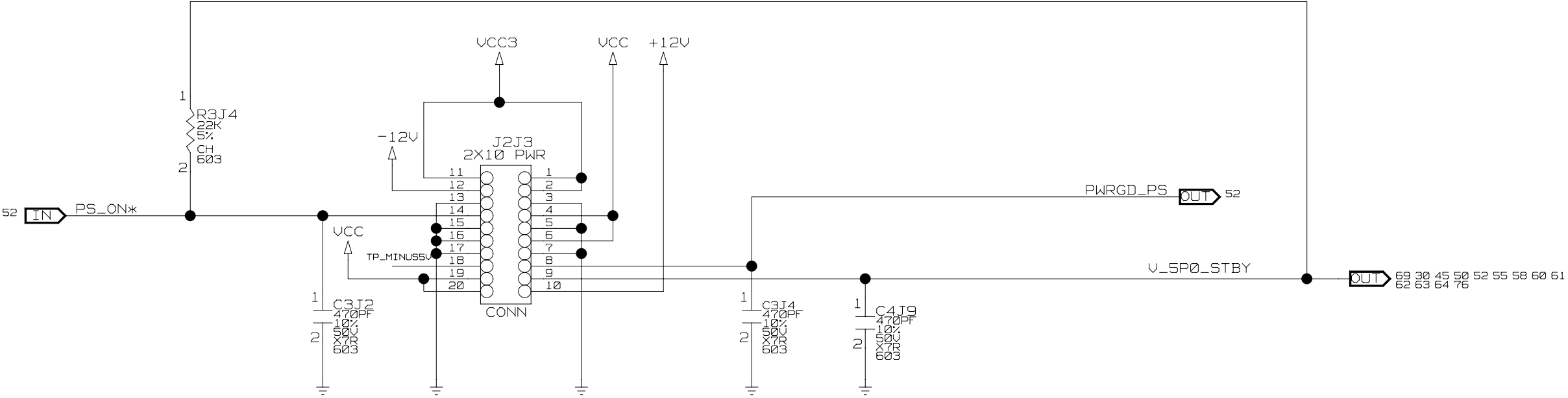


[PAGE_TITLE=2P5_VREG]

DRAWING

Mon Nov 18 13:52:21 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	59	4.0



STANDARD POWER CONNECTOR

DRAWING FAB_A.SCH.1.60
Mon Nov 18 13:52:30 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	60	4.0

D

C

B

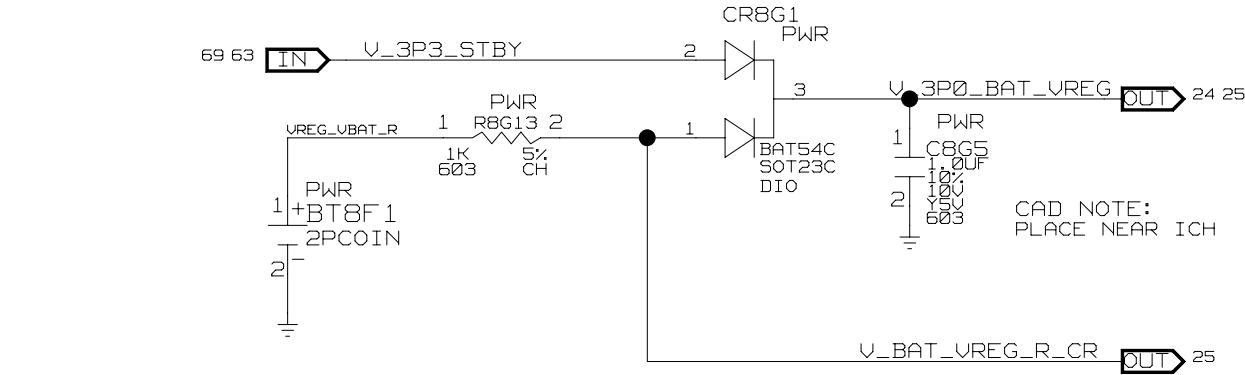
A

D

C

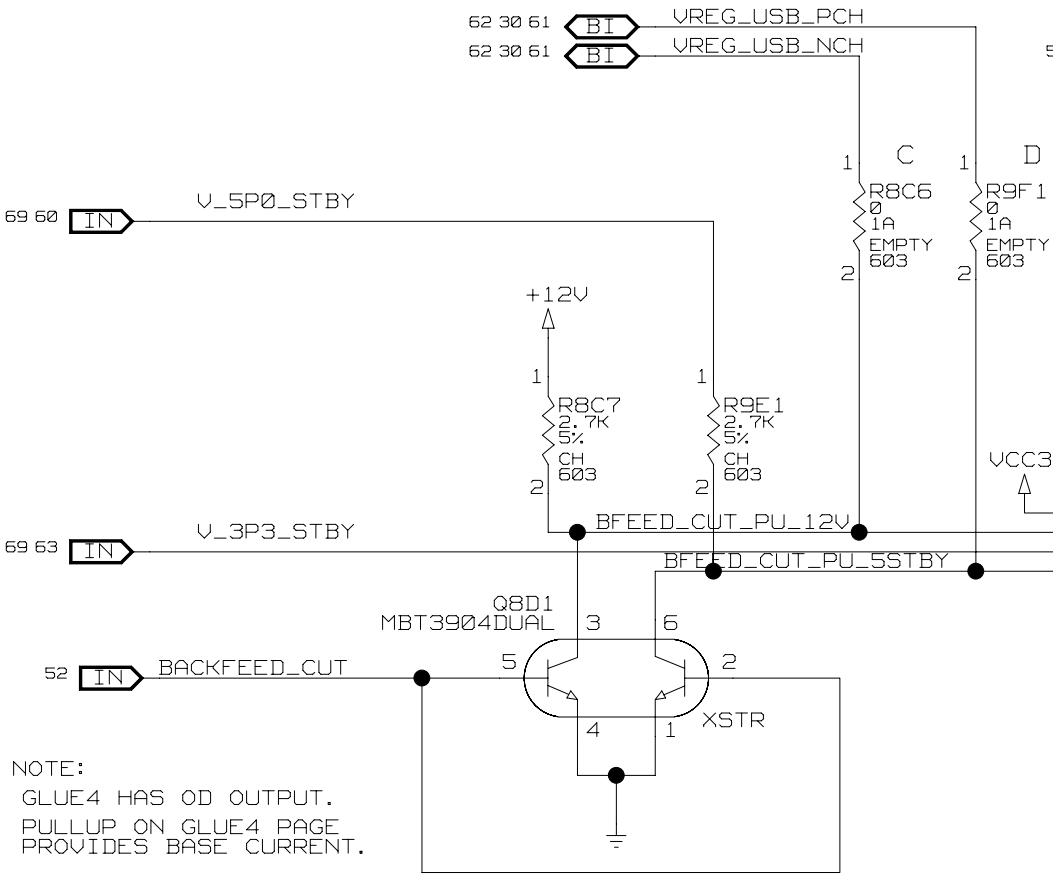
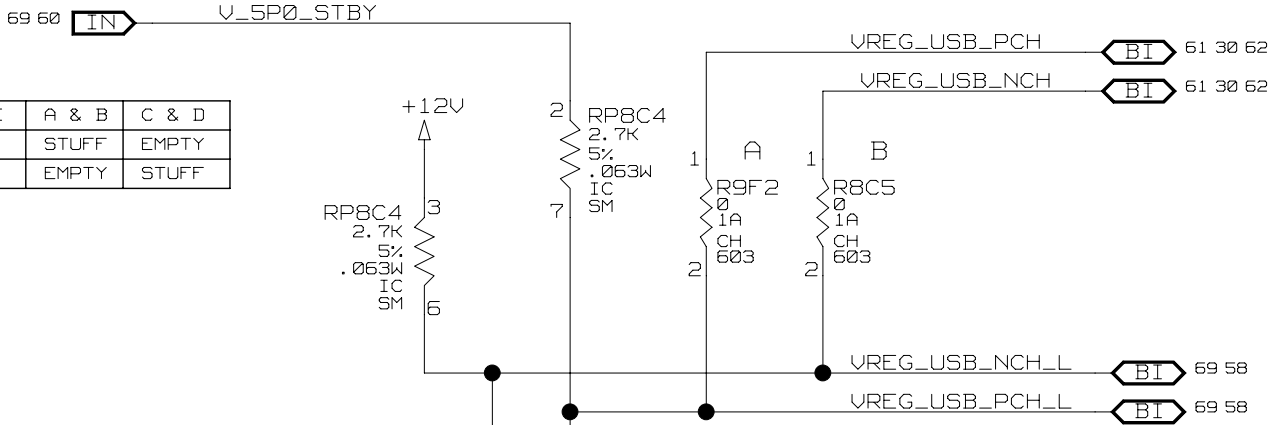
B

A

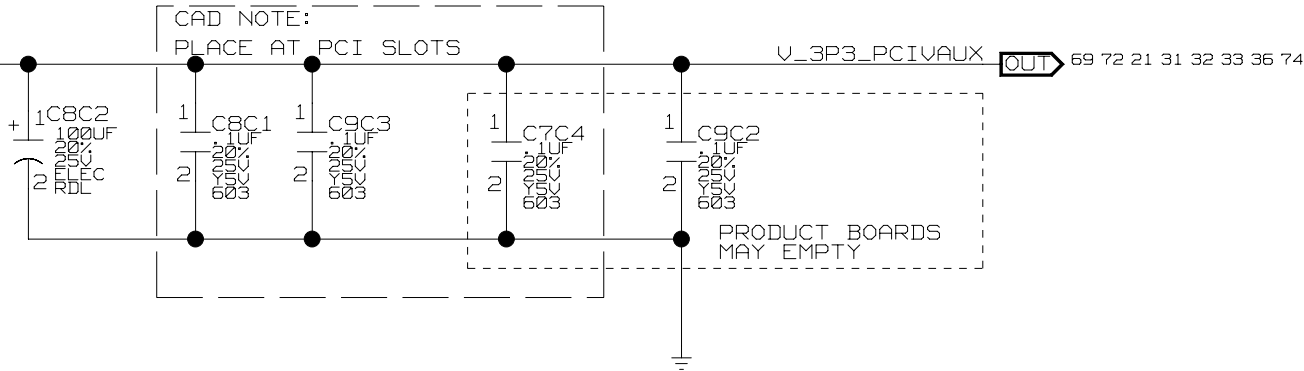


THROUGH-HOLE
CAD NOTE: DO NOT PLACE BATTERY NEAR
MOUNTING HOLES; GROUND OR VIAS

USB/PS2 WAKE	A & B	C & D
S3 ONLY	STUFF	EMPTY
S3, S4, S5	EMPTY	STUFF



NOTE:
GLUE4 HAS OD OUTPUT.
PULLUP ON GLUE4 PAGE
PROVIDES BASE CURRENT.

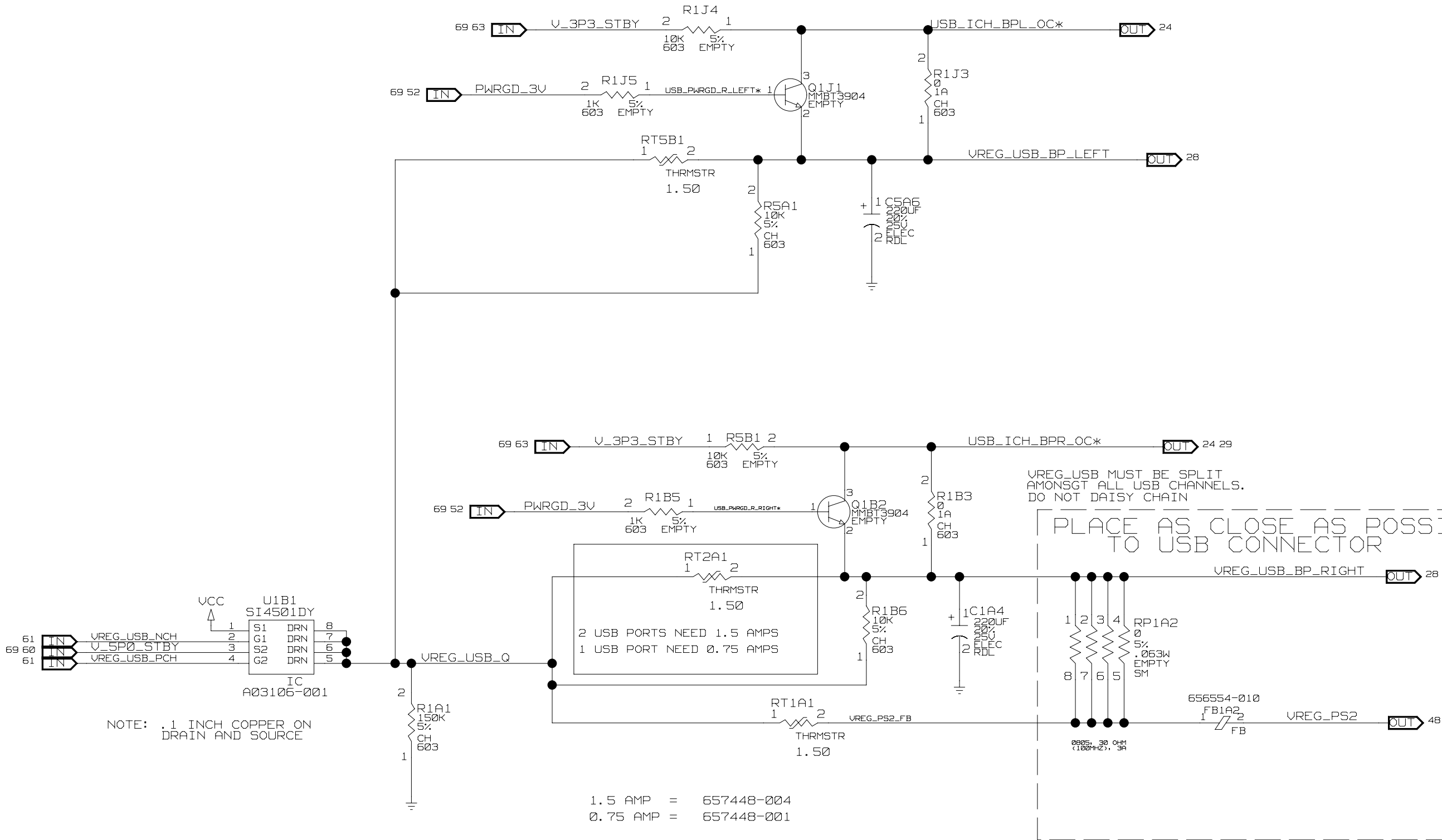


PCI VAUX

DRAWING

FAB_A.SCH.1.61
Mon Nov 18 13:52:39 2002
D845GFT FAB_A

DOCUMENT NUMBER
C23021
PAGE
61
REV
4.0

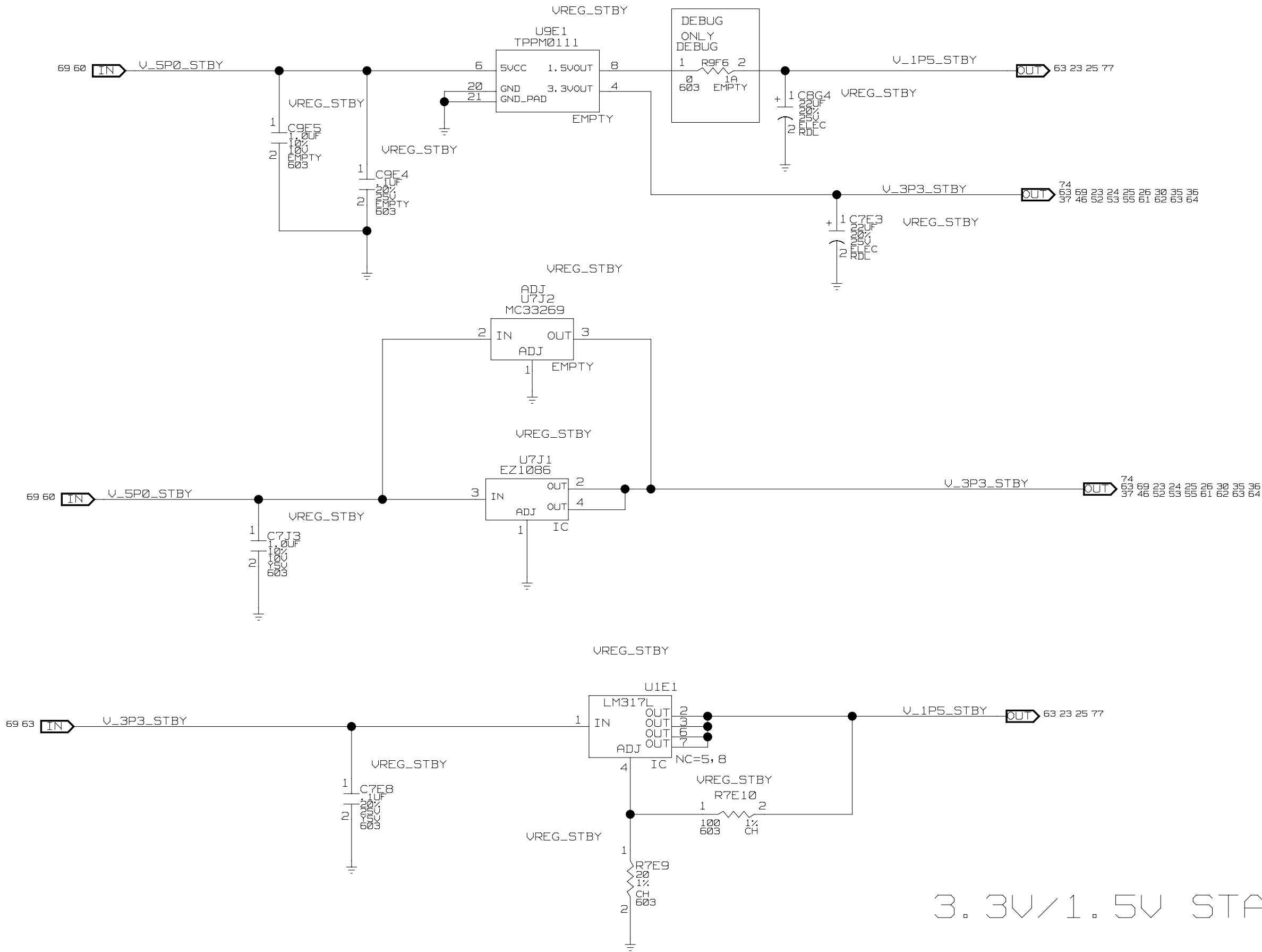


DRAWING

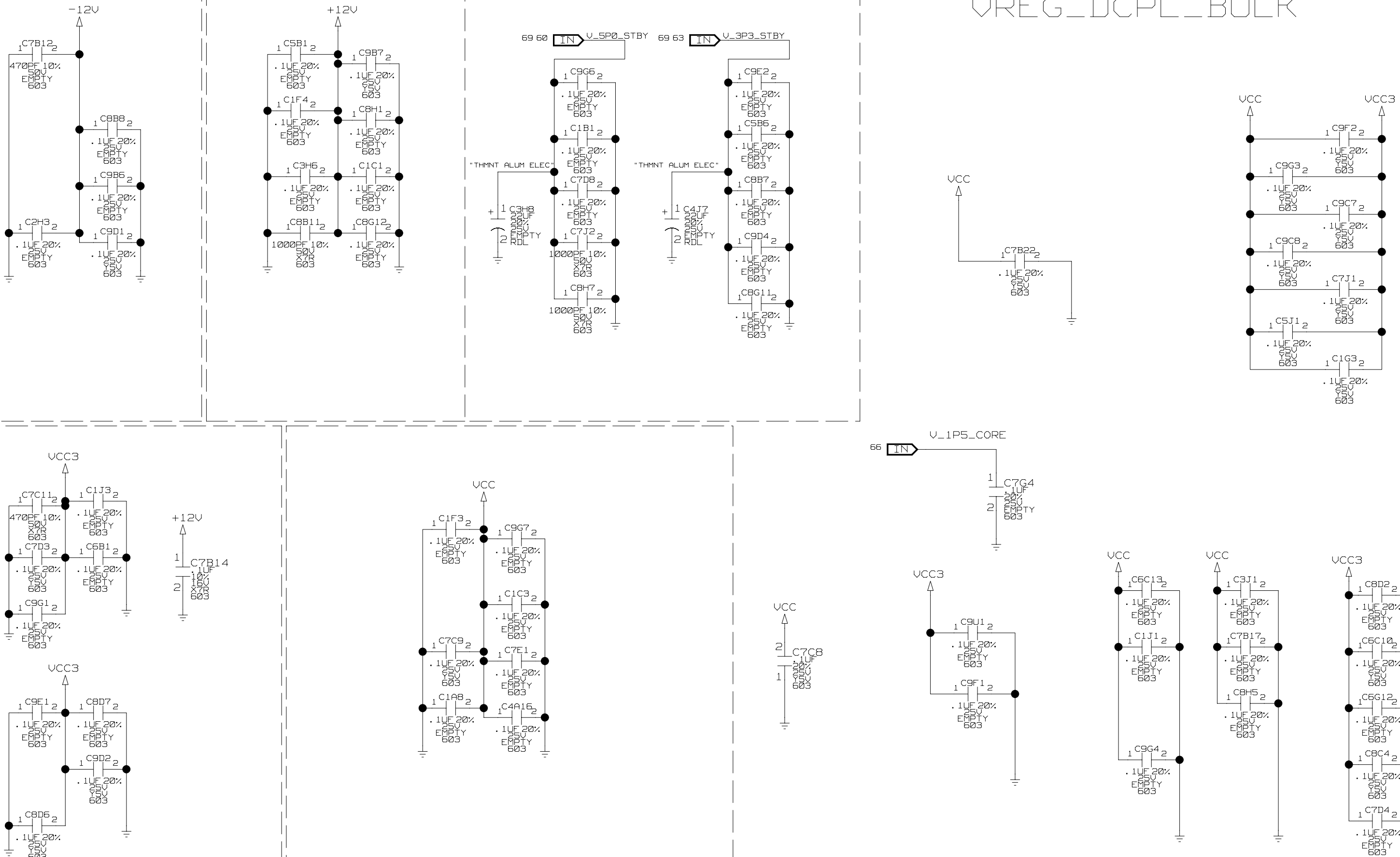
WAKE ON USB & PS2

FAB_A.SCH. 1.62
Mon Nov 18 13:52:48 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	62	4.0

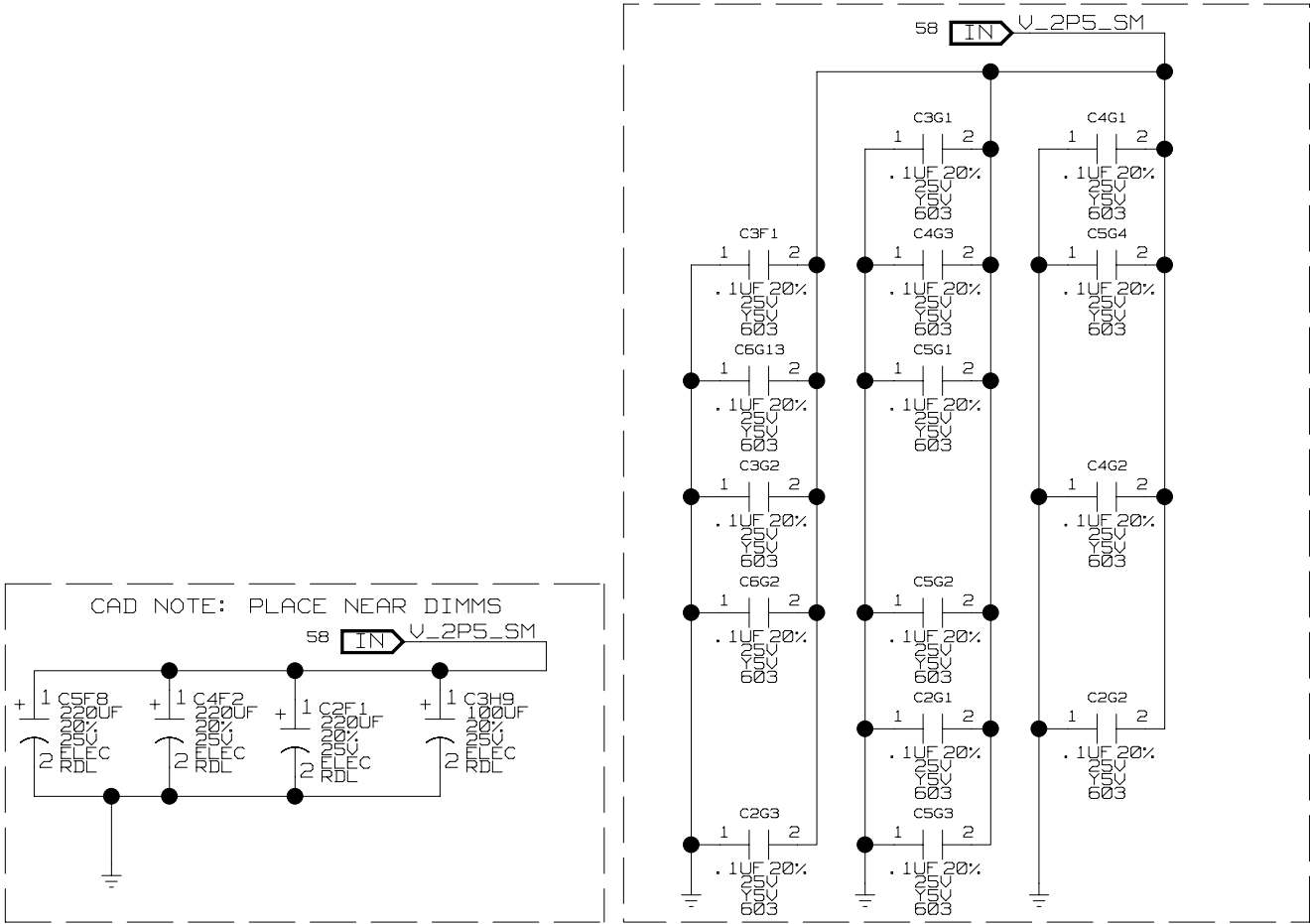


VREG_DCPL_BULK



ROOM=DCL_DDR_DCPL

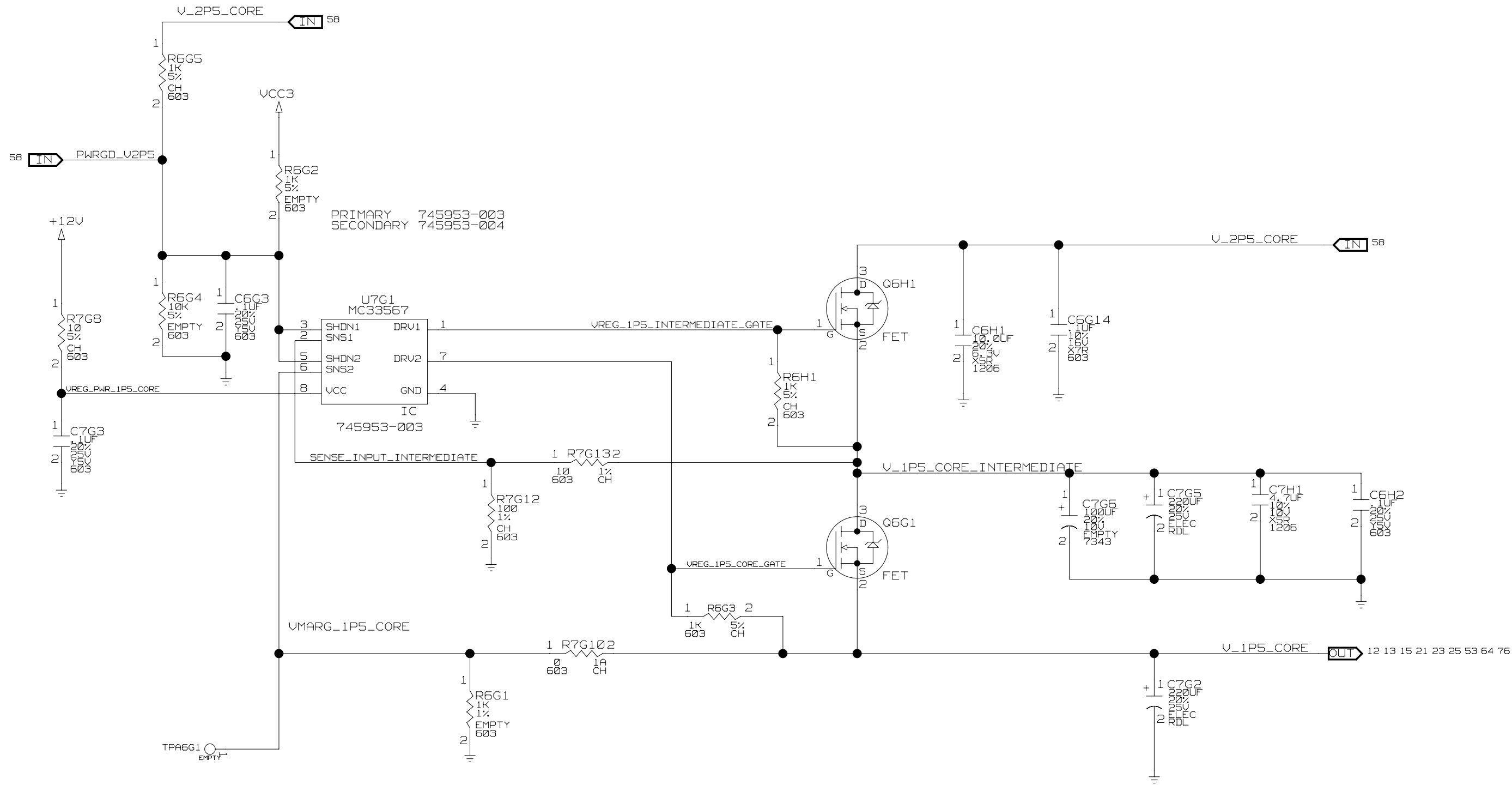
DDR 2P5_SM DECOUPLING



DRAWING

FAB_A.SCH. 1.65
Mon Nov 18 13:53:07 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	65	4.0



[PAGE_TITLE=1.5_VREG]

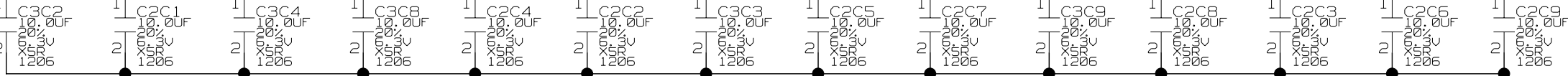
DRAWING

FAB_A.SCH.1.66
Mon Nov 18 13:53:17 2002
D845GFT FAB_A

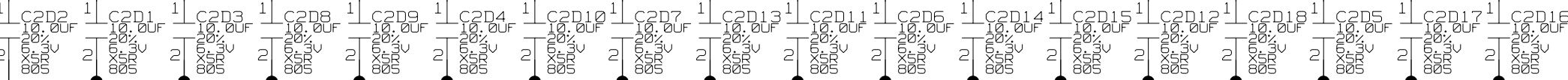
DOCUMENT NUMBER	PAGE	REV
C23021	66	4.0

ROOM = DCL_CORE_CPU_VREG

69 67 IN VCCP



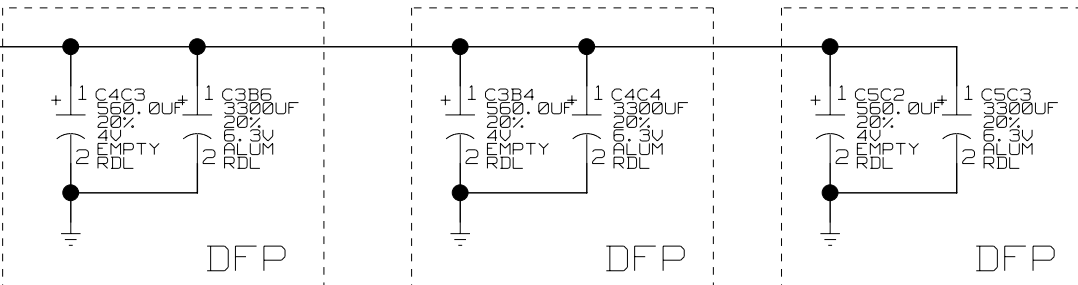
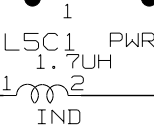
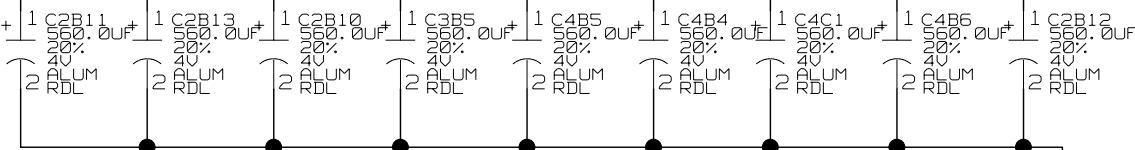
NOTE: PLACE THESE NORTH OF THE CPU SOCKET



NOTE: PLACE THESE IN THE CAVITY OF THE CPU SOCKET



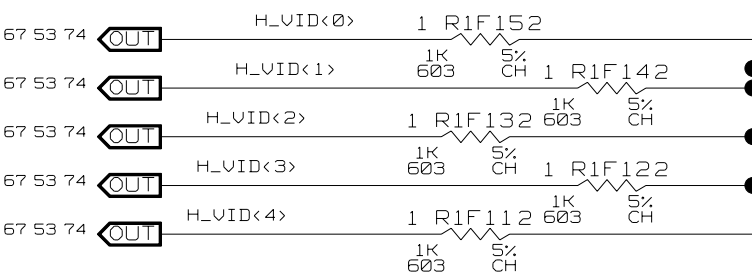
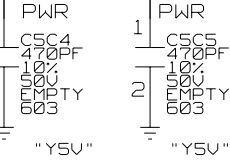
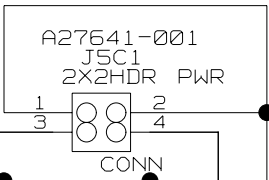
NOTE: PLACE THESE SOUTH OF THE CPU SOCKET



VREG_12V_FILTERED

OUT 67

VREG_12V_POWER OUT 69 57 67 74



VCC3

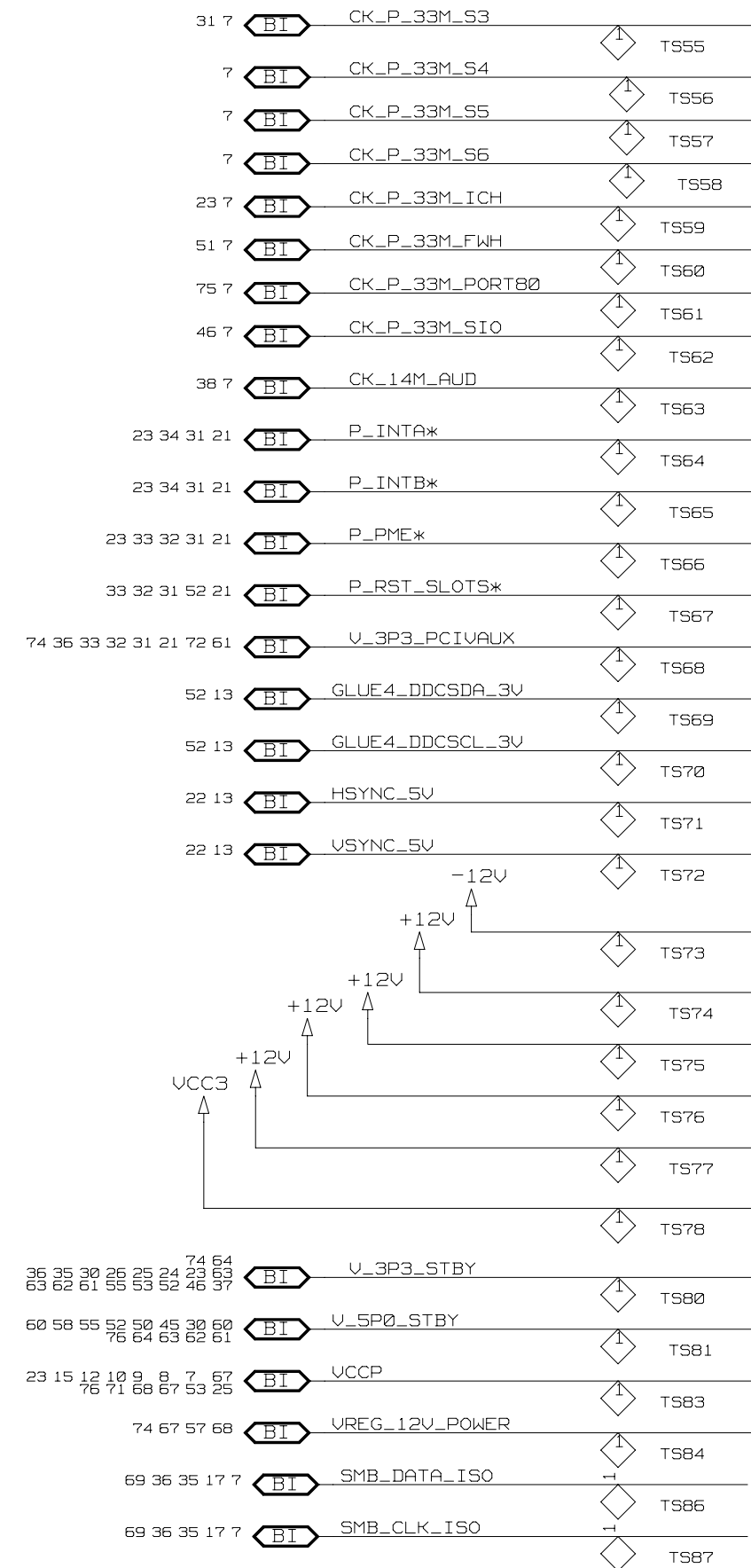
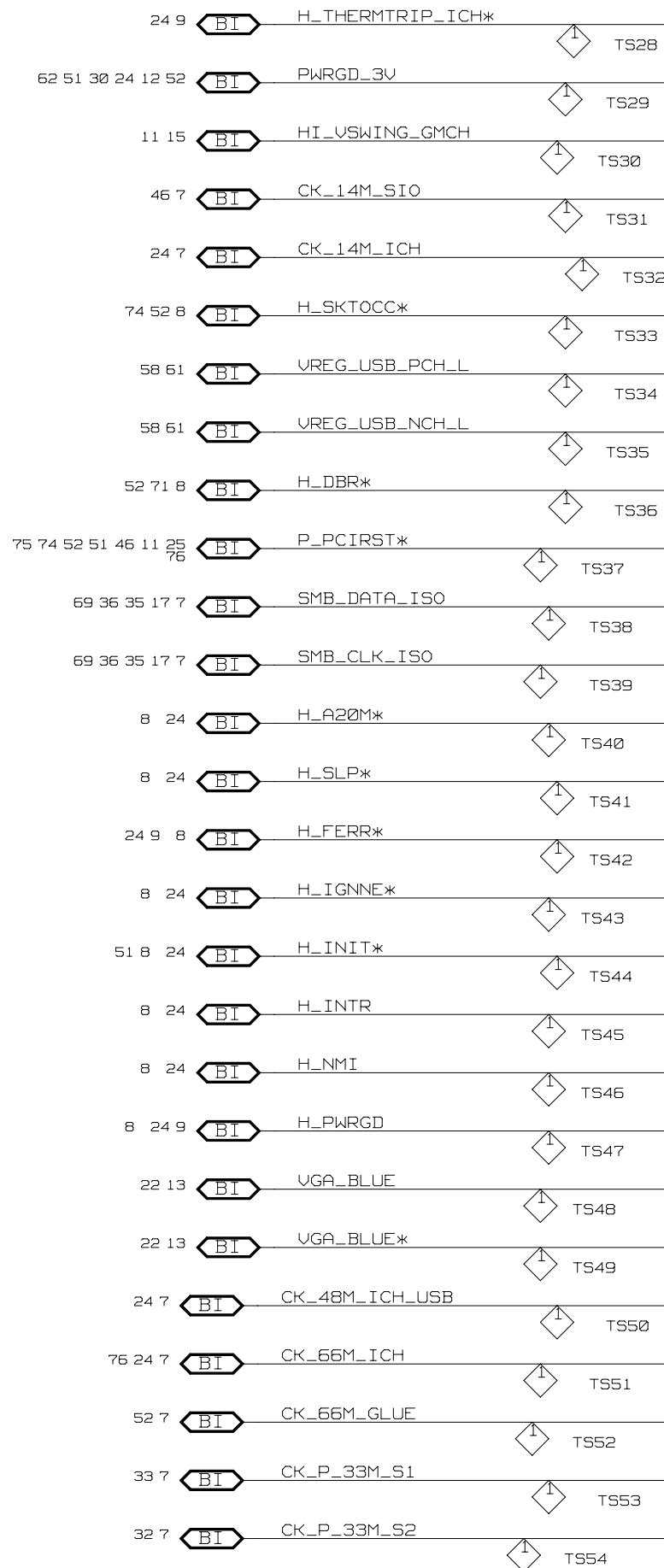
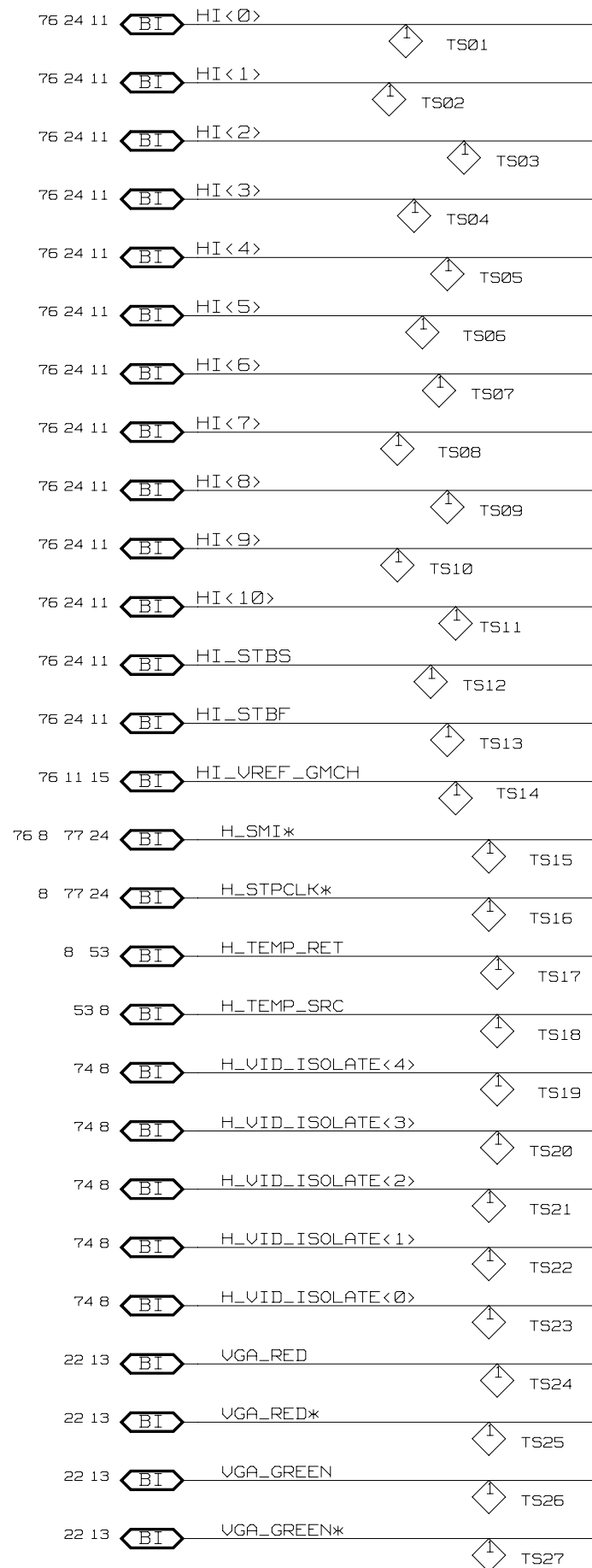
CAPACITORS

[PAGE_TITLE=CPU_VREG]

DRAWING FAB_A.SCH. 1.68
Mon Nov 18 12:32:53 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	68	4.0

ROOM=DCL_TRACK_SPLIT



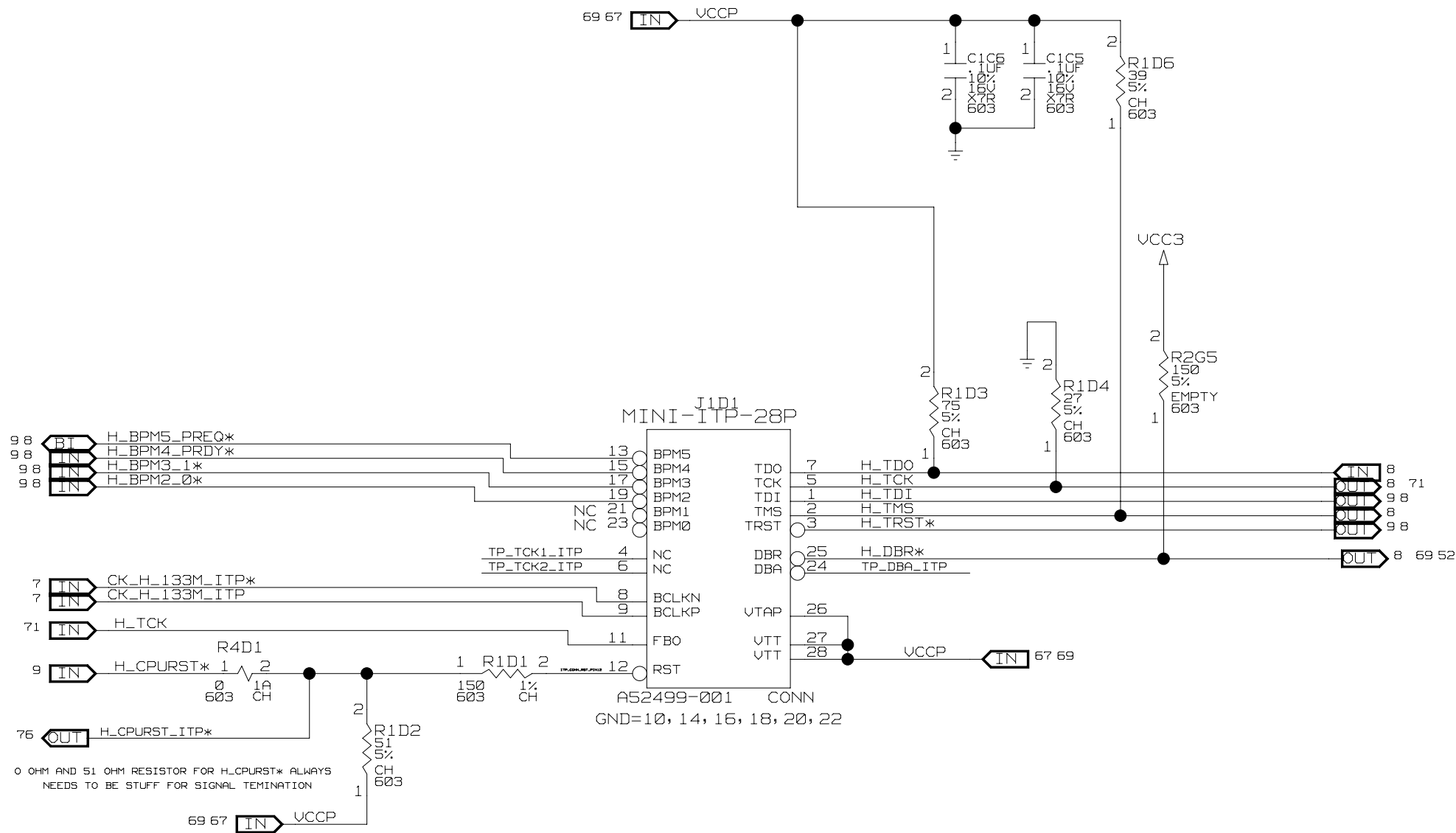
DRAWING FAB_A.SCH.1.69
Mon Nov 18 13:56:16 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	69	4.0

[MODULE=CORES]

CR-708		7	6	5	4	3	2		1
D									
C									
B									
A									
DEBUG PAGES									
DRAWING FAB_A.SCH.1.70 Mon Nov 18 12:47:56 2002 D845GFT FAB_A									
[DONOR_REV=1.02/page 41] [MODULE=VREG]		[PROJ_REV=2.00/page 70]		[SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2]		[PAGE_TITLE=VREG_VCCP_CAP_DECOUPLING]		[LAST_MAKEPROJ: 10/32/2001 1:57:13 PM]	
[DONOR_PROJ=NBVV_DDR--1130]		[PROJ_NAME=_G_DDR--1164]		[MODULE=VREG]		[MOD_PAGE=PAGE3]		[MOD_REV=REV0_2D]	
								2	
								1	

ITP 700FLEX CONNECTOR



CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN. FBO LENGTH = TCK + BPM LENGTHS TO CPU.
SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

CAN THE ITP HANDLE A 5VSB PULLUP ON DBR

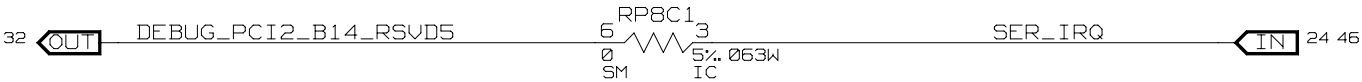
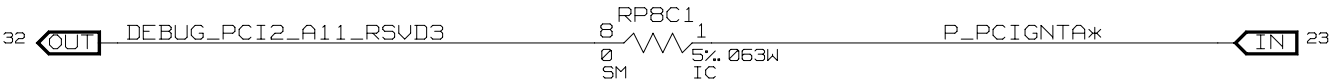
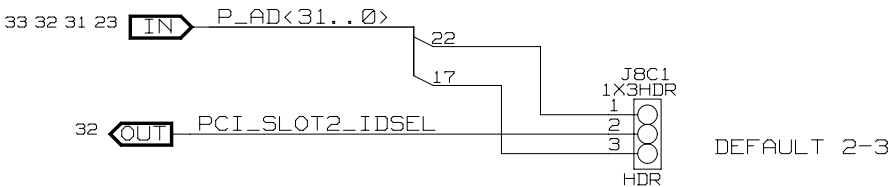
DRAWING
FAB_A.SCH.1.71
Mon Nov 18 13:55:25 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	71	4.0

DEBUG HOOKS MOON ISA



J8B3/J8C1	PCI SLOT 2 MODE
1-2	MOON ISA
2-3	PCI (DEFAULT)



[PAGE_TITLE=MOON_ISA]

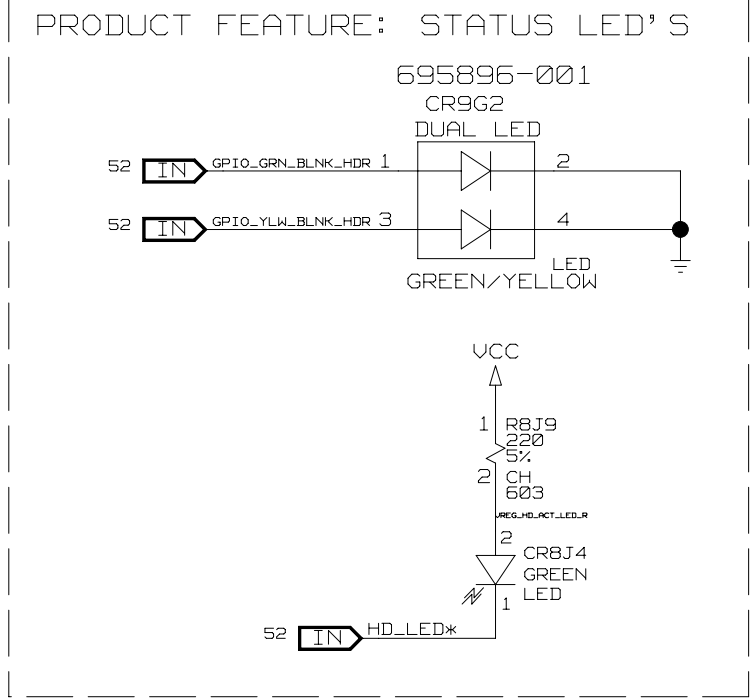
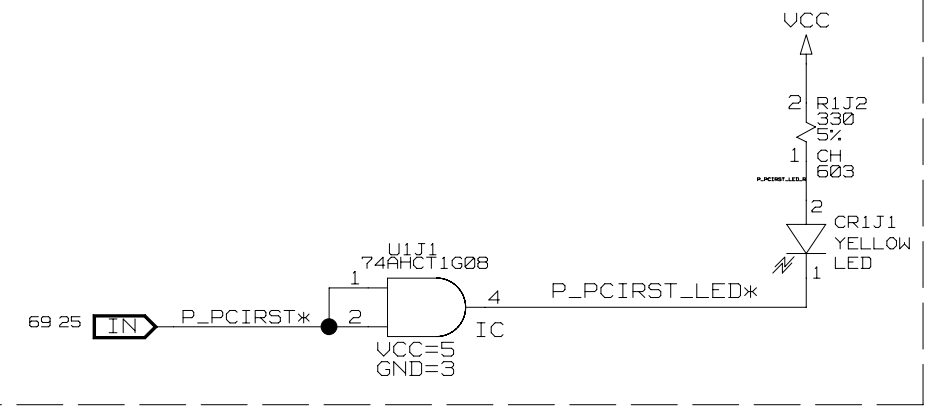
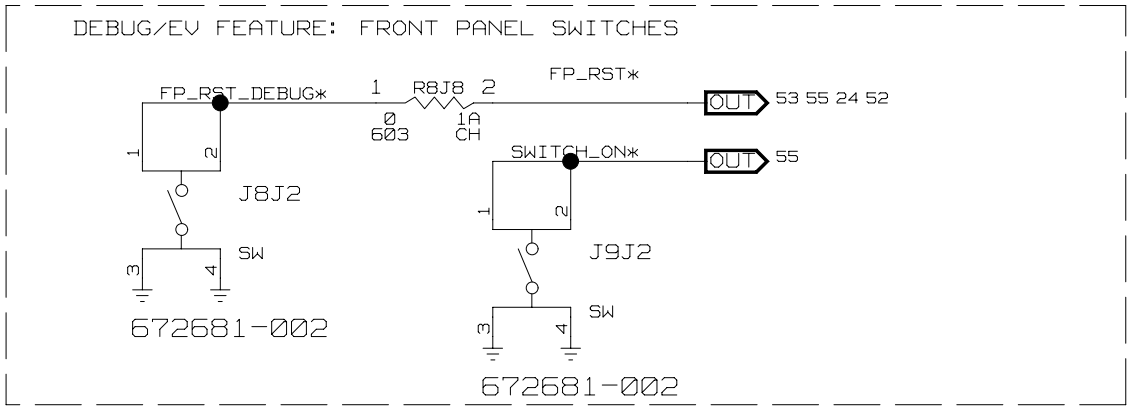
DRAWING

FAB_A.SCH. 1.72
Mon Nov 18 12:33:26 2002
D845GFT FAB_A

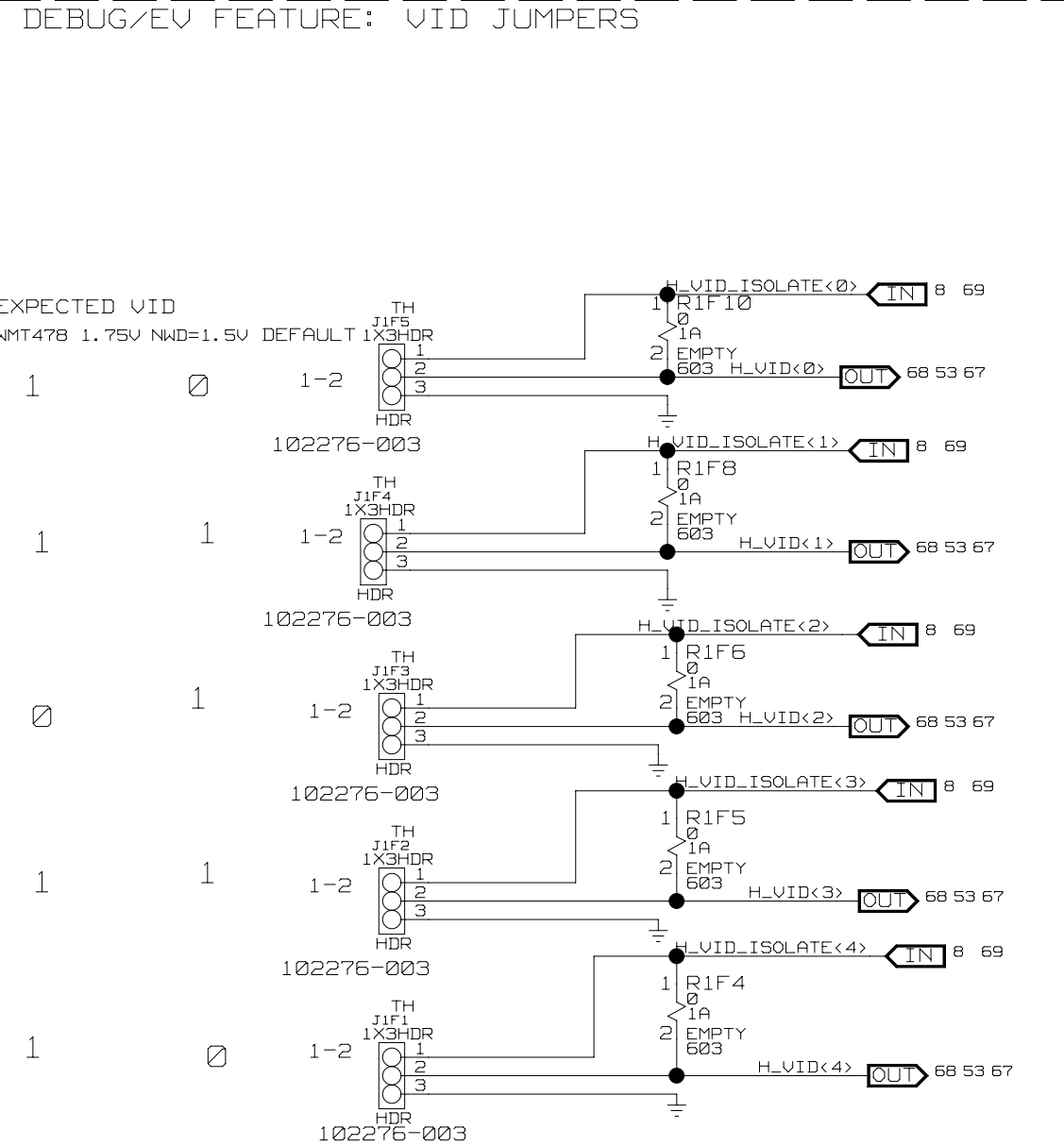
DOCUMENT NUMBER	PAGE	REV
C23021	72	4.0

CR-73 8		7	6	5	4	3	[FULL_ID=1164-79-16545][PAGE_INFO_ID=16545][TOWNED_BY=DEJ]		[MODULE_ID=128-19-14110][DONOR_ID=1130-76-15278]		
D											
C											
INTETIONALLY LEFT BLANK											
B											
A											
[PAGE_TITLE=BACKSIDE]											
DRAWING											
FAB_A.SCH.1.73											
Mon Nov 25 12:50:15 2002											
D845GFT FAB_A											
[LAST_MAKEPROJ: 10/13/2001 1:57:14 PM]											
2											
1											
[DONOR_REV=1.02/page73]		[PROJ_REV=2.00/page73]		6		5		4		3	
[DONOR_PROJ=NBVV_DDR--1130]		[PROJ_NAME=_G_DDR--1164]		[MODULE=NONE]							

D



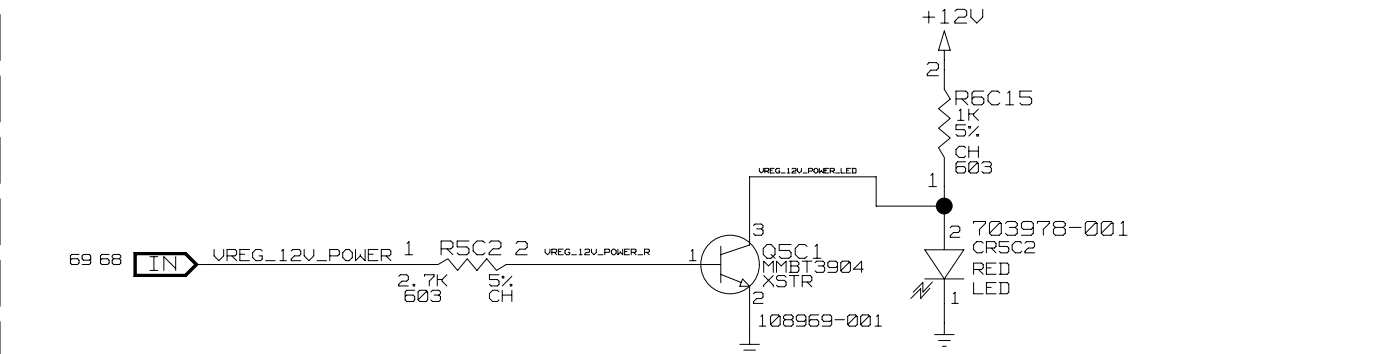
C



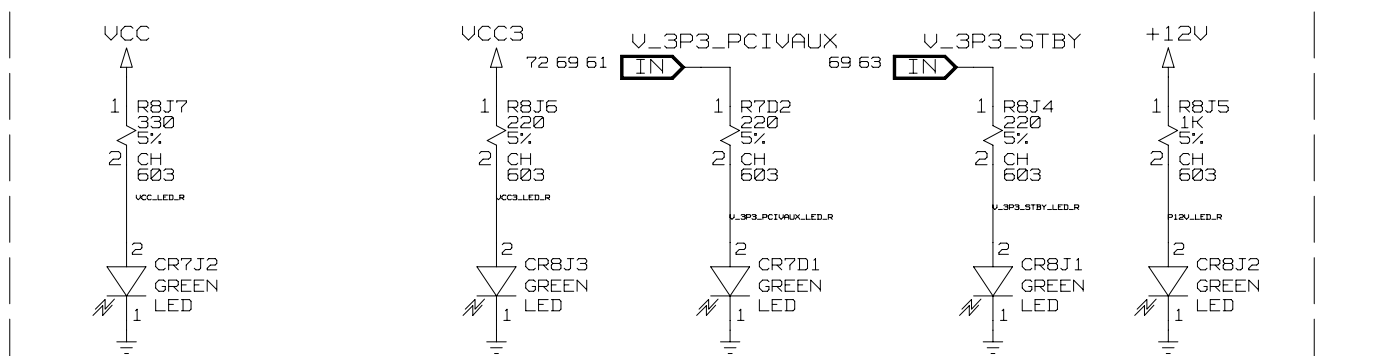
VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	1	1	1	1	OFF
1	1	1	1	0	1.1
1	1	1	0	0	1.125
1	1	1	0	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.25
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

B

DEBUG/EV FEATURE: RED WARNING LED ON CPU 12V CONNECTOR



DEBUG/EV FEATURE: POWER RAIL STATUS LED'S



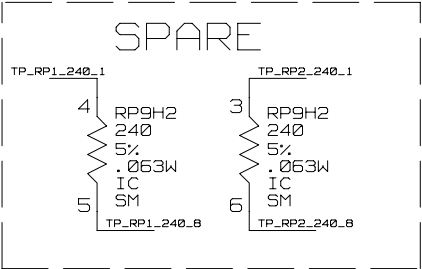
A

DESIGN NOTE: VID JUMPER FUNCTION

	JUMPER POSITION	
EV CARD?	1-2	2-3
YES	AVOID	FORCE 0
NO	CPU DRIVES	FORCE 0

[PAGE_TITLE=DEBUG_LED_DISPLAY]

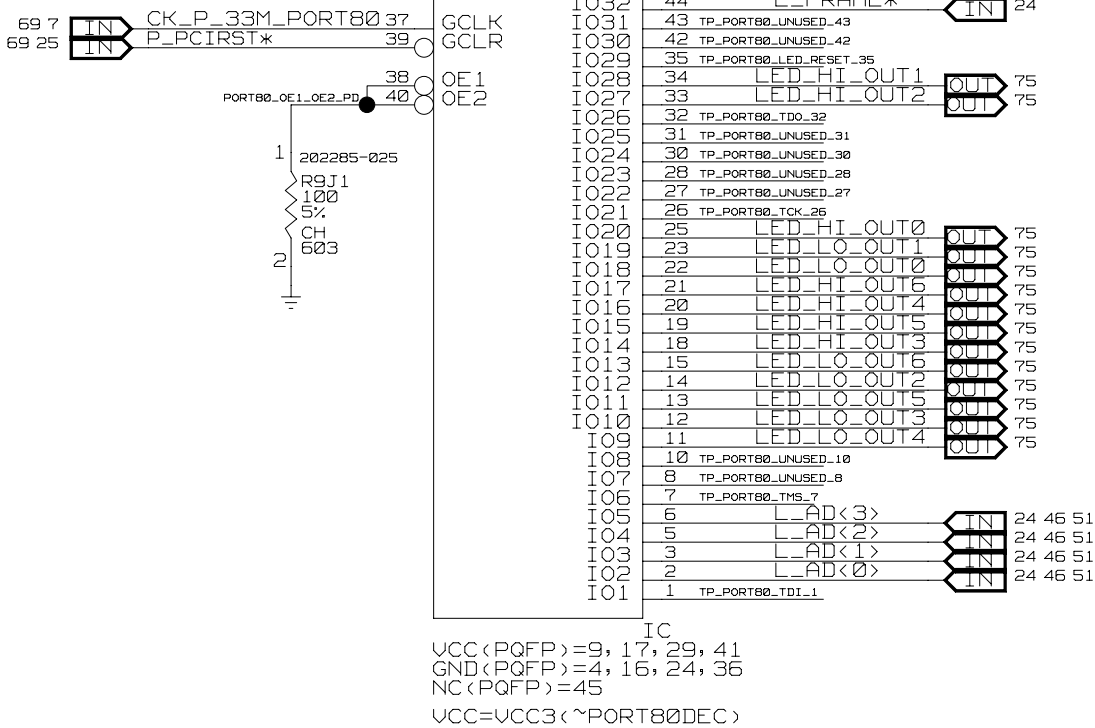
DRAWING
FAB_A.SCH.1.74
Mon Nov 18 13:56:44 2002
DB45GFT FAB_A



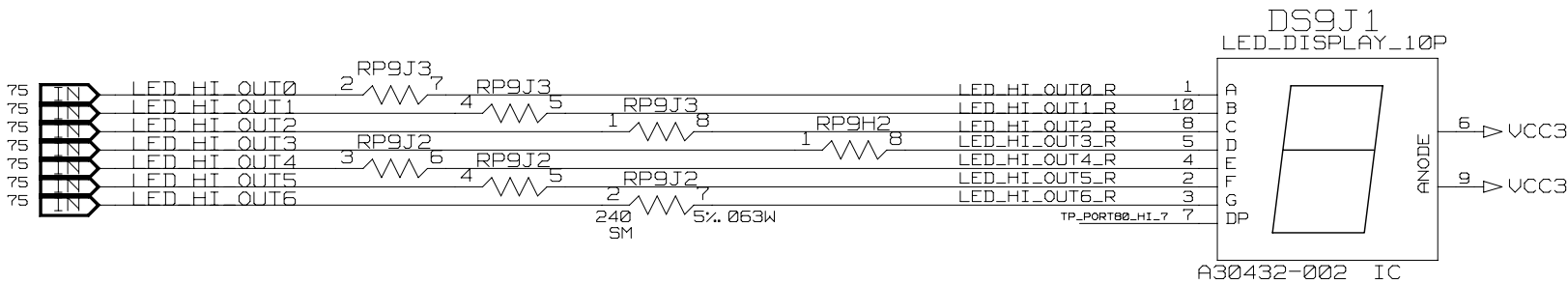
BLANK PART NUMBER: 3.3V COMPATIBLE (IPN XXXXXX-XXX)
PROGRAM FILE FROM D.E.SUBMITTED TO VENDOR
PROGRAM PART NUMBER & PLD-FA: A38794-001

EPM7032AETC44-10
44 PIN TQFP

U9J1
EPM7032 A38794-001

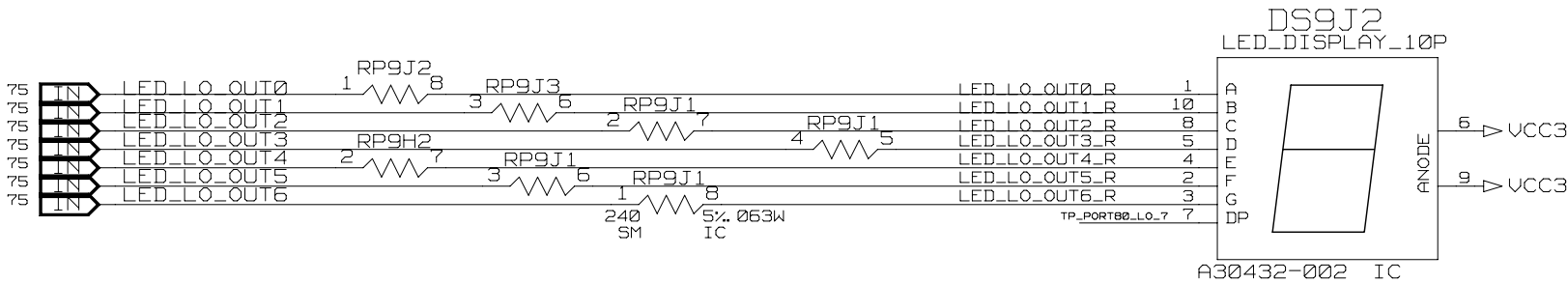


CAD NOTE: ORIENT TO LEFT

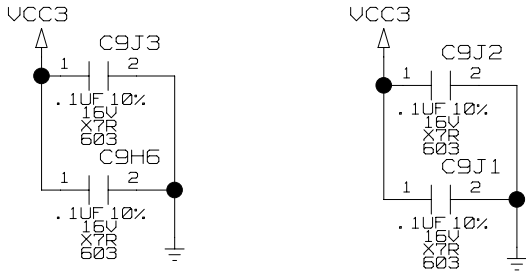


ALL RPACKS 240 OHMS

CAD NOTE: ORIENT TO RIGHT



CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY



DEBUG/EV FEATURE: PORT 80 DECODER & DISPLAY

DRAWING

FAB_A.SCH.1.75
Mon Nov 18 13:56:54 2002
DB45GFT FAB_A

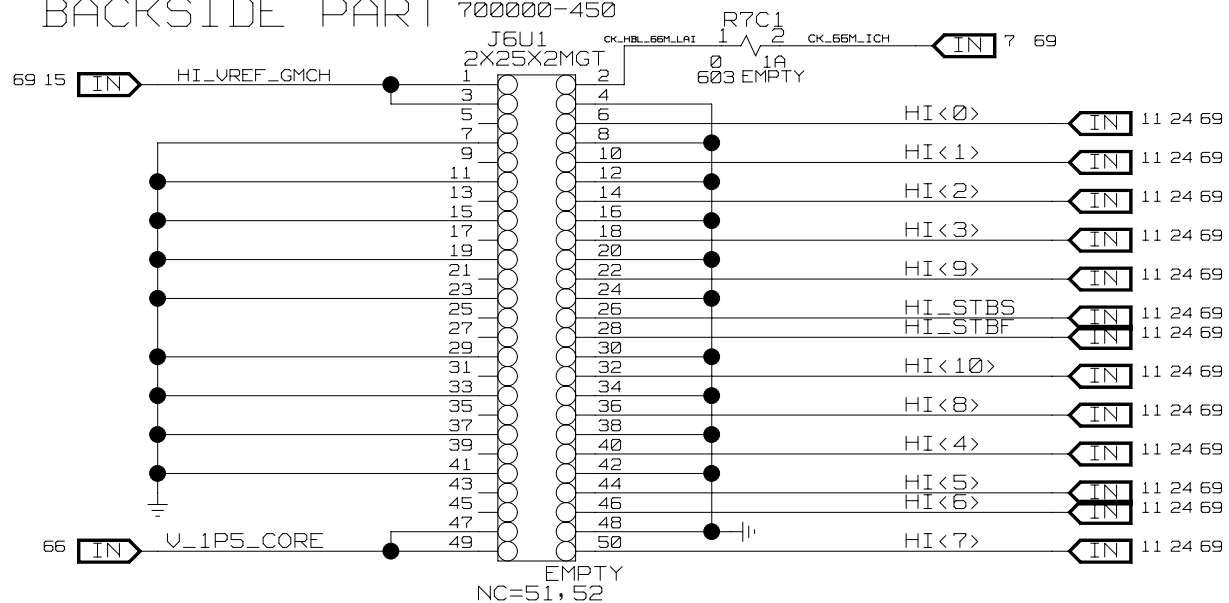
[PAGE_TITLE=LPC_DEBUG_PORT_80]

DOCUMENT NUMBER	PAGE	REV
C23021	75	4.0

DEBUG/EV FEATURE: HUBLINK LAI HEADER

NOTE: BACKSIDE PART 700000-450

PLACE AT MIDPOINT OF HUBLINK ROUTING

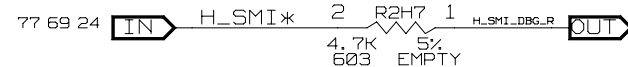
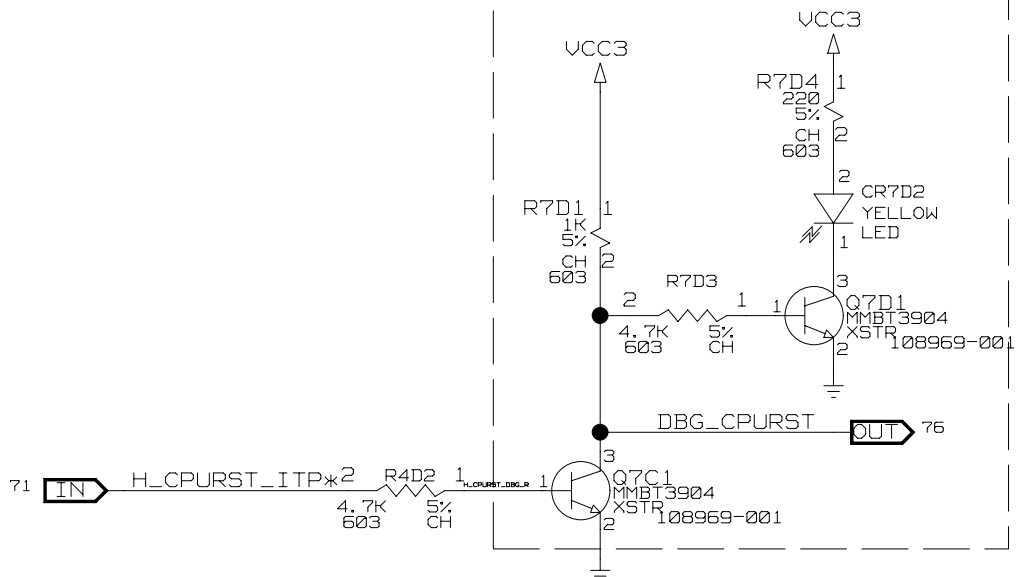
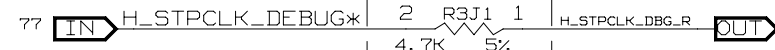


SOLDER MASK PADS: 5, 9, 13, 17, 21, 25, 27, 31, 35, 39, 43, 45
PINS ARE NOT ASSIGNED TP SIGNAL NAMES <PREVENTS TRACE CONNECTION>

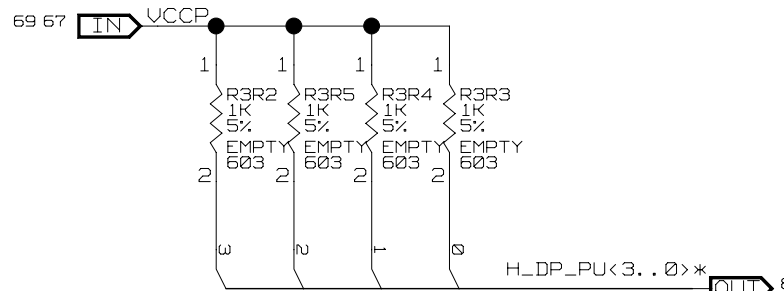
DEBUG/EV FEATURE: TDR COUPONS



DEBUG/EV FEATURE: INVERTING LEVEL SHIFTERS ON FSB SIGNALS FOR DIAG LED'S

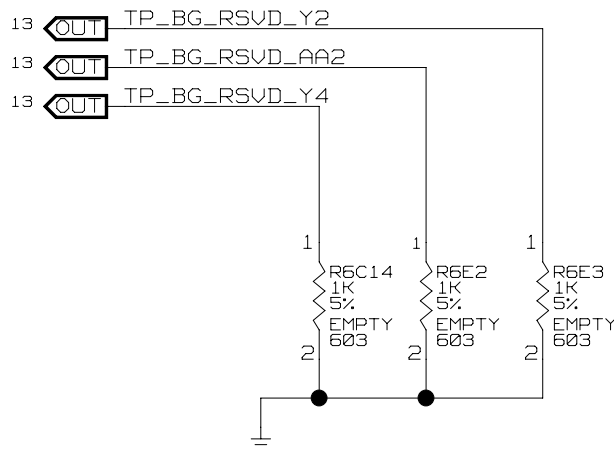
CAD NOTE:
PLACE UNDER DIMMSCAD NOTE:
PLACE BY CPU

DEBUG/EV FEATURE: BACKSIDE RESISTIVE TEST LOAD SITES



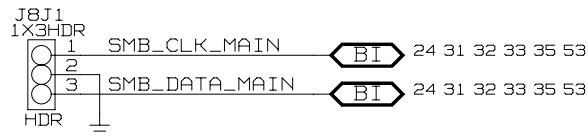
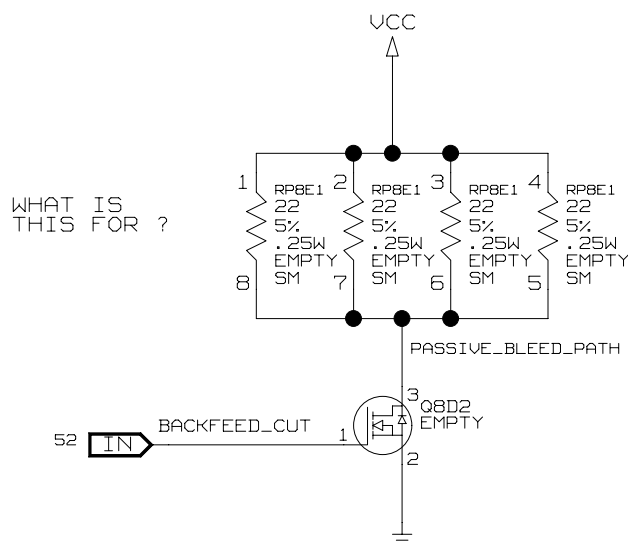
CAD NOTE: PLACE ON BACKSIDE, KEEP DP TRACE SHORT

DEBUG/EV FEATURE: GMCH PILOT MODE STRAPS.

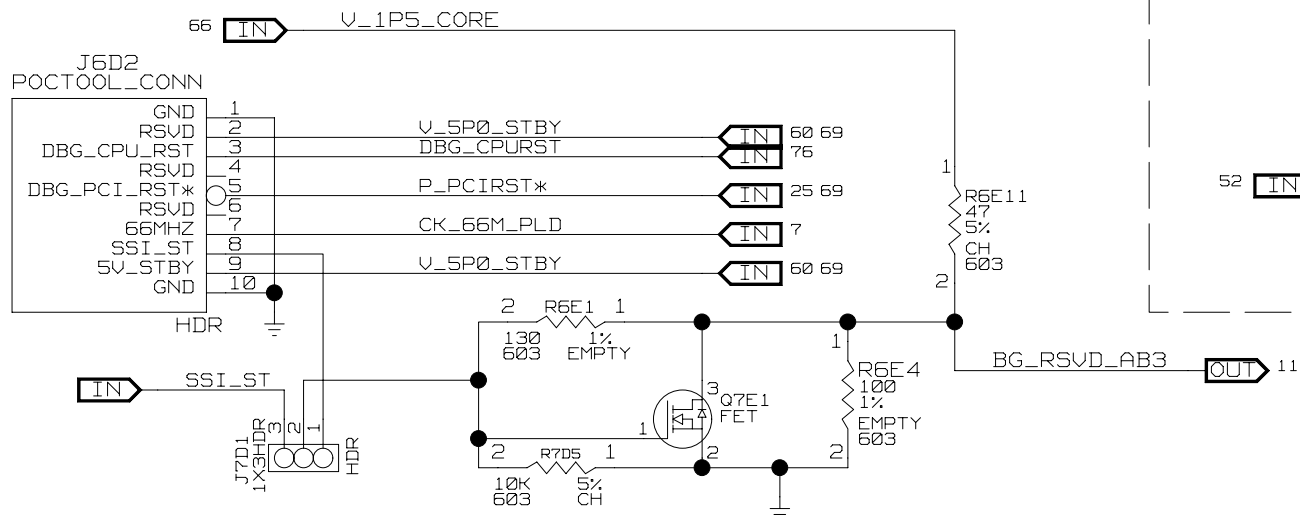


GMCH PIN #	
PILOT_8	Y8
PILOT_7	AA4
PILOT_6	W7
PILOT_5	AA5
PILOT_4	AA3
PILOT_3	Y4
PILOT_2	AA2
PILOT_1	Y2
PILOT_0	Y3

DEBUG/EV FEATURE: SMBUS LAI HEADER

CUSTOMER C
PASSIVE BLEED CIRCUIT

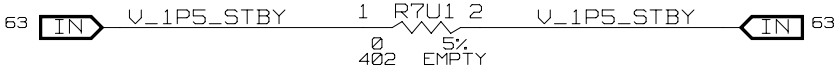
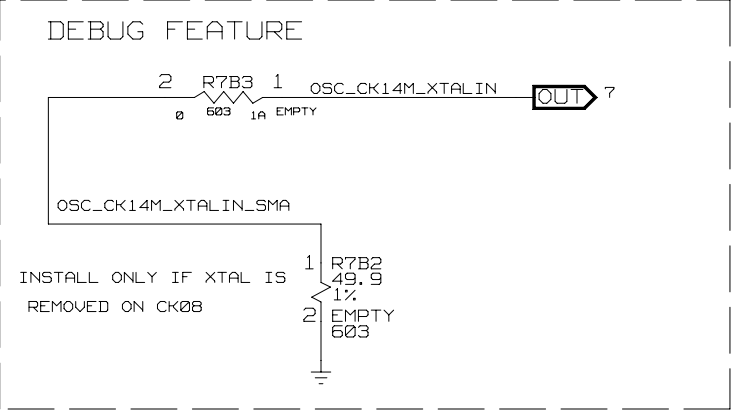
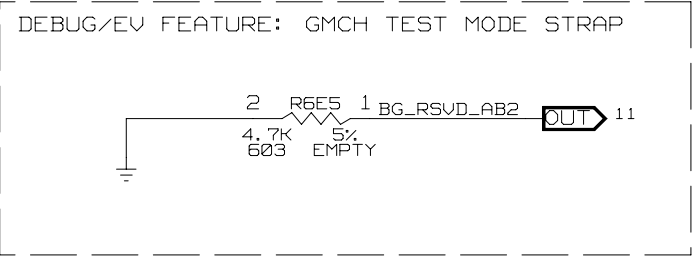
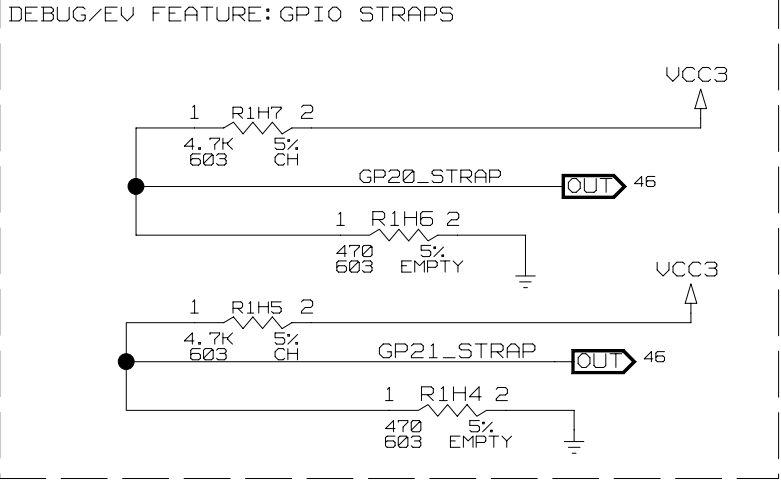
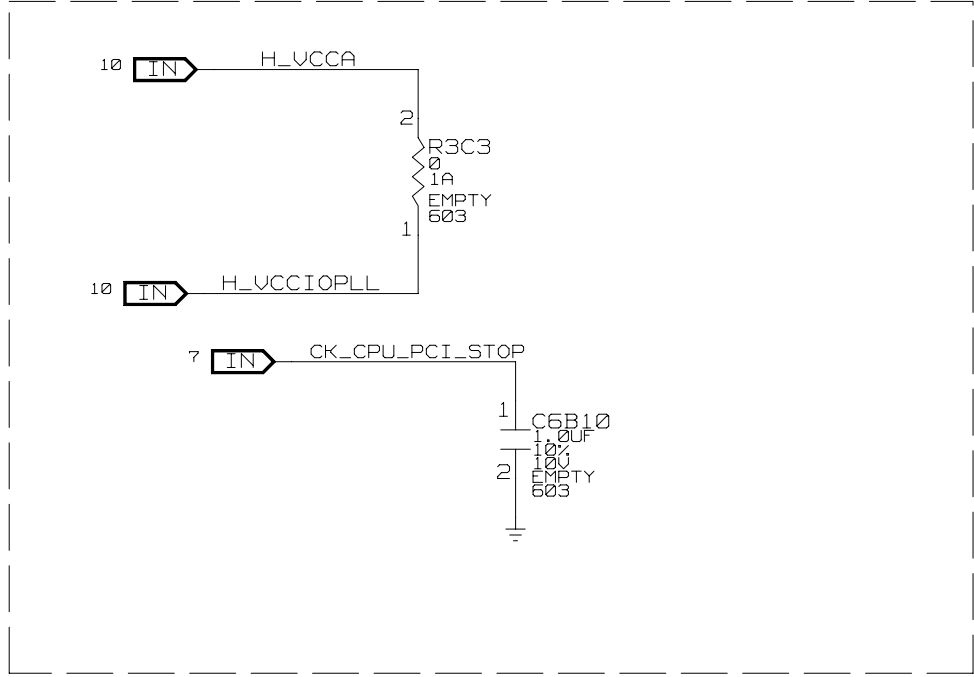
WHAT IS THIS FOR ?



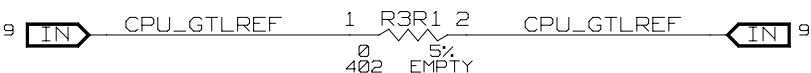
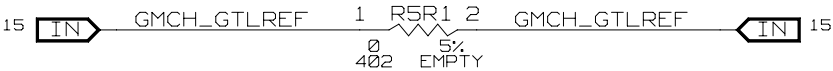
DRAWING

FAB_A.SCH.1.76

Mon Nov 18 13:57:06 2002
D845GFT FAB_ADOCUMENT NUMBER
C23021PAGE
76REV
4.0



ICH4 E20 BYPASS



DRAWING

FAB_A.SCH. 1.77
Mon Nov 18 12:34:45 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	77	4.0

[PAGE_TITLE=DEBUG_HEADERS]